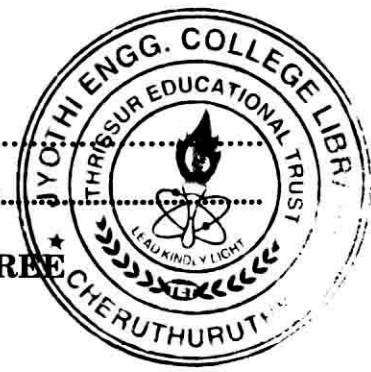


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Name.....

Reg. No.....



**SIXTH SEMESTER B.TECH. (ENGINEERING) DEGREE
EXAMINATION, APRIL 2014**

(2009 Scheme)

AI 09 L03—DIGITAL DESIGN WITH VHDL

[Regular/Supplementary/Improvement]

Time : Three Hours

Maximum : 70 Marks

Part A

Answer all questions.

Each question carries 2 marks.

1. Differentiate between MOD and REM.
2. Give the use of attributes in VHDL.
3. What do you meant by delta delay ?
4. What is a component ?
5. Write the syntax to change the default encoding of "TYPE state is (s0, s1, s2, s3)" (Assume the new encoding as : s0 = 11, s1 = 10, s2 = 01, s3 = 00).

(5 × 2 = 10 marks)

Part B

Answer any four questions.

Each question carries 5 marks.

6. Write a VHDL code for 2 × 1 MUX using CASE.
7. What are the logical operators defined in VHDL give examples.
8. Distinguish between Concurrent statements and Sequential statements.
9. Design a 3 bit binary up counter in VHDL.
10. Write notes on resolving functions include examples.
11. Explain BIST with a Generic BIST scheme.

(4 × 5 = 20 marks)

Part C

Answer all questions.

Each question carries 10 marks.

12. (a) Write a VHDL code to model a 7-level priority encoder.

Or

- (b) Design a generic parity detector circuit in VHDL.

Turn over

13. (a) Write a function to overload the "+" (addition operator) to allow the direct addition of STD_LOGIC_VECTOR value.

Or

- (b) (i) Compare functions and procedures. (4 marks)
(ii) Write notes on inertial and transport delay mechanisms include appropriate examples. (6 marks)

14. (a) Design an n bit ripple adder in VHDL, with full adder unit as a component for the design.

Or

- (b) Design a 4 bit comparator in VHDL with appropriate components declared in a package (State assumptions clearly).

15. (a) Write notes on (i) Boundary scan ; (ii) Predefined attributes.

Or

- (b) Write a test bench for a full adder circuit (The input vectors are to be read from infile1.txt and output is stored in outfile1.txt).

(4 × 10 = 40 marks)