63002

Name : .....

Reg. No: .....

SEVENTH SEMESTER B.TECH (09 Scheme) DEGREE SUPPLEMENTARY EXAMINATION, APRIL 2014

AI 09 704 - ANALOG AND DIGITAL CIRCUIT DESIGN

Time:Three Hours **Maximum : 70 Marks**

Part A

1. What is a Current Mirror?
2. Give the expression for the voltage gain of a Common-Gate stage with a current-source load.
3. Define Slew Rate of an Operational Amplifier.
4. Name the two types of associations used in VHDL structural modelling.
5. Write the VHDL code for a tristate buffer using **IF** statement.

(5x2=10 Marks)

Part B

Answer any four questions

6. Compare common source, common drain and common gate amplifiers.
7. Briefly explain the second order effects of MOS.
8. Explain the operation and advantages of folded cascode amplifiers.
9. Derive the expression for the output of a summer and integrator.
10. What are package declaration and package body? Explain with suitable examples.
11. Explain PLA and PAL with suitable examples.

(4 x 5 = 20 Marks)

Part C

12. Derive an expression for the frequency response of a Cascode amplifier.

(or)

13. Derive an expression for the drain current of MOS and its terminal voltages. Also sketch its VI characteristics.
14. Explain miller compensation and derive an expression for the miller compensation.

(or)

15. (i) Explain the advantages of switched capacitor implementation. (ii) State the characteristics of an ideal operational amplifier.
16. Discuss in detail about Generics and configurations with suitable examples.

(or)

17. With suitable examples explain the following sequential statements
    (i) Exit
    (ii) Next
    (iii) Assertion
    (iv) Report.
18. Write the VHDL code for a Full Adder using (i) structural Modeling and (ii) Dataflow modeling.

(or)

19. Design a BCD to excess-3 code converter and write the VHDL code using structural modelling.

(4x10 = 40 Marks)

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