D 51035 (Pages : 2) Name.....

Reg. No.....

THIRD SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, NOVEMBER 2013

IT/CS 09 306—SWITCHING THEORY AND LOGIC DESIGN

Time : Three Hours Maximum : 70 Marks

Part A

Answer **all** *questions.*
Each question carries 2 *marks.*

1. Convert the decimal 108.364 to a binary number.
2. Define parity.
3. What is a PLA ?
4. Give *two* applications for counter.
5. What is a latch ?

(5 × 2 = 10 marks)

Part B

Answer any **four** *questions.*
Each question carries 5 *marks.*

6. Simplify using Boolean algebra
   $(A+\bar{B})(A+C)$ and $AB + (\bar{A}+\bar{B})C + AB$.
7. State and explain DeMorgan's theorem.
8. Explain the operation of 3-to-8 decoder.
9. Differentiate multiplexer and demultiplexers.
10. Write notes on fault classes.
11. Explain the operation of parallel-in parallel-out shift register.

(4 × 5 = 20 marks)

Part C

Answer **all** *questions.*
Each question carries 10 *marks.*

12. (a) Using Karnaugh map method, simplify the following expressions to minimum sum-of-products form :
    $X = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}C$ and $X = \bar{A}(BC + B\bar{C}) + A(BC + B\bar{C})$.

Or

(b) Explain the simplification using Quine-McClusky method.

Turn over

13. (a) Explain the operation to look-ahead adders.

Or

(b) Draw the truth table for 4-to-16 decoder and explain its operation.

14. (a) Explain the procedure for detecting fault using path sensitization method.

Or

(b) Explain Boolean difference method with suitable example.

15. (a) Draw the timing diagram of a two three bit asynchronous binary counter and explain.

Or

(b) Describe the working of a 4-bit Johnson counter.

(4 × 10 = 40 marks)