D 50624 (Pages : 2) Name.....

Reg. No.....

FIFTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION
NOVEMBER 2013

EE/PTEE 09 505—DIGITAL SYSTEM DESIGN

Time : Three Hours Maximum : 70 Marks

Part A

Answer **all** *the questions.*

1. What are test benches ?
2. Brief on WAIT statement.
3. Draw the schematic of any two types of 3-state buffers.
4. Differentiate between state table, state diagram and state equation.
5. What are feedback sequential circuits ?

(5 × 2 = 10 marks)

Part B

Answer any **four** *questions.*

1. What are test benches ?
2. How are package declaration made in VHDL ?
3. Explain the importance of tri-state devices.
4. What is state minimization ?
5. Define races and hazards.
6. Write a note on switch matrix of XC 9500 CPLD.

(4 × 5 = 20 marks)

Part C

Answer **all** *the questions.*

1. (a) Explain with example how timing analysis is performed in VHDL.

   (b) Define the three styles of modelling in VHDL with simple example.

Or

2. (a) Write a note on libraries and packages in VHDL by giving suitable examples.

   (b) What are the different types of loop statements available ? Explain.

Turn over

3. (a) Write VHDL code for a parity generator.

   (b) How are tri-state devices modelled in VHDL ?

Or

4. Write the VHDL code for a 4-bit magnitude comparator.

5. Design a synchronous sequential circuit with one input x and one input z that recognizes input sequence σ_1 . Use DFF's for realization.

Or

6. Draw the state diagram of serial binary adder and design the sequential circuit.

7. Draw the ASM chart for a 3-bit odd parity generator and discuss its features.

Or

8. Explain the IO block of XC 4000 FPGA.

(4 × 10 = 40 marks)