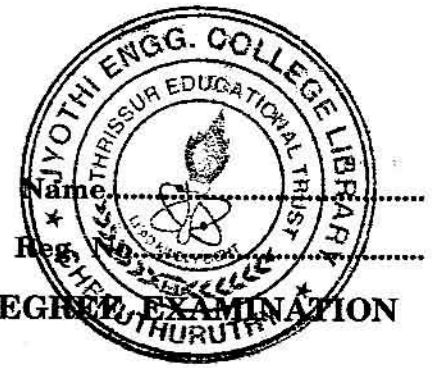**D 51030**   (Pages : 2)

THIRD SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION NOVEMBER 2013

EC 09 305/PTEC 09 304—DIGITAL ELECTRONICS

Time : Three Hours

Maximum : 70 Marks

Part A

Answer all questions.

1. Find 1010100–1000011 using 1's complement.

2. Convert $(7265 \cdot 45)_{10}$ to octal.

3. Simplify $(B\bar{C} + \bar{A}D)(A\bar{B} + C\bar{D})$ to a minimum number of literals.

4. Write the concept of SR flip-flop.

5. Draw the basic blocks of ASM chart.

(5 × 2 = 10 marks)

Part B

Answer any four questions.

6. Simplify $F(A,B,C,D,E) = (0, 2, 4, 6, 9, 13, 21, 23, 25, 29, 31)$.

7. Implement $F(x, y, z) = \Sigma(0, 6)$ with NAND gates.

8. Construct adder cum subtractor.

9. Implement $F(A, B, C, D) = \Sigma(0, 1, 3, 4, 8, 9, 15)$ with a multiplexer.

10. Convert D flip-flop to T flip-flop with a combinational logic.

11. Write the importance of ASM chart.

(4 × 5 = 20 marks)

Part C

Answer section (a) or section (b) of each question.

12. (a) Simplify using Quine–Mc Clusky method

$P(A, B, C, D, E, F, G) = \Sigma(6, 9, 13, 18, 19, 25, 27, 29, 41, 45, 57, 61)$.

Or

Turn over

(b) Simplify the following functions and implement them with two level NOR gate circuits.

(i) $F = w\bar{x} + \bar{y}\,\bar{z} + \bar{w}\,y\,\bar{z}$.

(ii) $F(w, x, y, z) = \Sigma\,(5, 6, 9, 10)$.

13. (a) Draw the logic diagram for a BCD to excess 3 code converter and explain.

Or

(b) Draw the TTL gate with totem-pole output and explain.

14. (a) Draw the universal shift register and explain.

Or

(b) Construct a 4-bit ripple up-down counter.

15. (a) Design a sequential circuit with two D flip-flops, A and B and one input x. When $x = 0$, the state of the circuit remains the same when $x = 1$, the circuit goes through the state transitions from 00 to 01 11 to 10 back to 00 and repeats.

Or

(b) Design a counter with the following repeated binary sequence with D flip-flops 0, 1, 2, 3, 8, 10, 13, 15.

(4 × 10 = 40 marks)