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Name.....

Reg. No.....

SEVENTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, NOVEMBER 2013

EC/PTEC 09 703—ANALOG AND MIXED MOS CIRCUITS

(2009 Scheme)

Time : Three Hours Maximum : 70 Marks

PART A (5X2 =10 MARKS)
ANSWER ALL QUESTIONS

1. State any two limitations of CMOS technology.
2. Draw the schematic of a current source.
3. Define stability of an Amplifier.
4. What is the significance of miller capacitance?
5. Define lock range and capture range of a PLL.

PART B (4X5 =20 MARKS)
ANSWER ANY FOUR QUESTIONS

6. Explain the working of a MOS transistor as a switch.
7. Explain the Small signal model of a MOS transistor.
8. Explain the working of any one high gain amplifier architecture.
9. Explain the noise analysis in single stage amplifiers.
10. What is the significance of Switched capacitor realization? Explain the switched capacitor integrator.
11. Explain the implementation of ladder filter using switched capacitors.

PART C (4X10=40 MARKS)
ANSWER ALL QUESTIONS

12. (a) (i) How active resistors are realized with MOS transistors? Explain.
(ii) Derive an expression for the R_{out} and V_{min} of a Cascode current mirror.

(or)

(b) Explain the working of a band gap reference.

13. (a) Derive the frequency response of a Differential amplifier.

(or)

(b) How Multipliers are configured with Gilbert Cells? Explain.

14. (a) Explain the steps involved in the design of single and two stage operational amplifiers.

(or)

(b) Discuss in detail about Folded Cascode amplifiers.

15. (a) Explain the working and non idealities of a Phase Locked Loops.

(or)

(b) Discuss in detail about the Comparator and its design.