D 51038 (Pages : 2)

Name.....

Reg. No.....

THIRD SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION NOVEMBER 2013

AI 09 305—DIGITAL SYSTEMS

Time : Three Hours Maximum : 70 Marks

Part A

Answer **all** *questions.*
Each question carries 2 *marks.*

1. What is a Parity bit ? List its types.
2. Distinguish between PLAs and PALs.
3. State any *two* advantages of CMOS Logic over other families.
4. State the difference between Mealy and Moore Machine.
5. What are the *two* types of Asynchronous sequential circuits ?

(5 × 2 = 10 marks)

Part B

Answer any **four** *questions.*
Each question carries 5 *marks.*

6. State and prove De Morgan's theorem.
7. Find the Canonical form of $f(A, B, C, D) = ABC' + AB'D + C'D + CD'$.
8. Write a brief note on ROM.
9. Explain the operation of a Jk flip-flop.
10. Explain the characteristics of ECL Logic.
11. What are cycles and races ? How are they avoided ?

(4 × 5 = 20 marks)

Part C

Answer any **four** *questions.*
Each question carries 10 *marks.*

12. (a) Reduce the following expression using K–Map :

$f(A, B, C, D, E) = \sum m(0, 2, 4, 15, 21, 27, 29) + \sum d(3, 5, 26)$.

Or

(b) Minimize :

$F(A, B, C, D) = \sum m(0, 1, 5, 7, 8, 9, 10, 11, 14, 15)$ using Quine McCluskey method.

Turn over

13. (a) Implement the following function using suitable multiplexers :

$F(A, B, C, D) = \sum m (0, 2, 4, 6, 8, 10, 12, 14)$.

Or

(b) Implement a full adder using suitable decoder and additional logic gates.

14. (a) Design a MOD-5 counter and explain its operation.

Or

(b) Explain the operation of a Monostable Multivibrator and astable multivibrator.

15. (a) Design a serial adder using Mealy state machine and explain its operation.

Or

(b) Minimize the state table given below :

Present State	*Next State*, Z (*Output*)	
	X *Input*	
	0	1
A	B, 0	C, 0
B	B, 0	D, 0
C	B, 0	C, 0
D	E, 1	C, 0
E	B, 0	D, 0

(4 × 10 = 40 marks)