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D 50566 (Pages : 2) Name.....

Reg. No.....

SEVENTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, NOVEMBER 2013

AI 09 704—ANALOG AND DIGITAL CIRCUIT DESIGN

(2009 Scheme)

Time : Three Hours Maximum : 70 Marks

Part A (5x2=10 Marks)

1. What does it mean channel is pinched off?

2. How is it possible to eliminate feed forward path through Miller capacitor in frequency compensated circuits?

3. If the clock frequency of parallel switched capacitor equivalent resistor is 100kHz, find the value of the capacitor C that will emulate a 1MΩ resistor.

4. Name the different data objects in VHDL

5. Check whether the following declarations are correct. If not make necessary corrections.

(i)Signal CLOCK: BIT

(ii)Variable COUNT: INTEGER

Part B (4x5=20Marks)

6. Draw the drain characteristic for a depletion mode transistor for different values of Vgs.

7. Explain switched capacitor integrator..

8. Draw the circuit diagram of CMOS sample and hold crcuit.

9. Differentiate between EXIT and NEXT statements.

10. Implement a half adder using structural modelling.

11. What is the function of Assertion statement in VHDL?

Part C (4x10=40 Marks)

12 (a) Draw and explain the C-V characteristic of a MOS structure.

OR

(b)Derive the gain and frequency response of a Differential Amplifier.

Turn over

13. (a) Draw the circuit diagram and explain the operation of a folded cascode amplifier.

OR

(b) Explain the MOS two stage amplifier in detail.

14. (a) Explain the different types of iteration schemes of using loop statements in VHDL.

OR

(b)Write short notes on (i) Generics (ii) Configurations.

15. (a) Model a 4-bit adder using generate statement.

OR

(b)Model a 4 bit serial in serial out shift register.