44785

Name : .....

Reg. No: .....

EIGHTH SEMESTER B.TECH (ENGINEERING) DEGREE EXAMINATION, AUGUST 2013

EC 04 801 – MICROELECTRONIC TECHNOLOGY
(2004 Scheme)

Time : Three Hours **Maximum : 100 Marks**

Part A

Answer all questions.

1. State and explain Flick's Law.
2. Explain deal-grove model.
3. Explain LOCOS.
4. What is the significance of multilevel metallization? Explain.
5. Compare CMOS and bipolar technologies.
6. What are the advantages and limitations of BiCMOS technology.
7. What is cell hierarchy? Explain.
8. Draw the layout of a CMOS Inverter.

(8 x 5 = 40 Marks)

Part B

Answer all questions.

9. (a) Explain the Wafer Processing Steps.

(Or)

(b) (i) Explain oxidation process.
(ii) Explain MOCVD and molecular beam epitaxy.

10. (a) Explain SILO and SWAMI process.

(Or)

(b) Explain the steps involved in SOI technology.

11. (a) Explain early and advanced bipolar processes.

(Or)

(b) Explain the Twin-Tub process.

12. (a) Explain the Lambda based layout design rules.

(Or)

(b) Draw the layout of CMOS NAND gate and explain the various layers.

(4 x 15 = 60 Marks)

******