C 44423 (Pages : 2) Name.....

Reg. No.....

SEVENTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, JUNE 2013

EC/PTEC 09 704—DIGITAL SYSTEM DESIGN

(2009 Admissions)

Time : Three Hours Maximum : 70 Marks

Part A

Answer **all** *questions.*

1. State the difference between Synchronous and Asynchronous sequential circuits.
2. What is an VHDL Attribute ?
3. State the difference between PROM, PLA and PAL.
4. Define clock skew.
5. What is an hazard ?

(5 × 2 = 10 marks)

Part B

Answer any **four** *questions.*

6. Briefly explain the *two* types of Asynchronous sequential circuits.
7. What are the *two* rules for state assignment ? Explain with suitable example.
8. Write the VHDL code for a 4 × 1 multiplexer using case statements in Behavioural modelling.
9. With suitable examples explain the differences between selected signal assignment statements and conditional signal assignment statements.
10 Design a 2-bit Magnitude comparator and realize its using suitable PLA.
11. Explain the Metastability behaviour of Flip-Flops.

(4 × 5 = 20 marks)

Part C

Answer **all** *questions.*

12. (a) Design an asynchronous sequential circuit with two inputs x_1 and x_2 and with two outputs z_1 and z_2 for the following specifications :

(i) When $x_1 x_2 = 00$, the output $z_1 z_2 = 00$.

(ii) When $x_1 = 0$ and x_2 changes from 0 to 1, the output $z_1 z_2 = 10$.

(iii) When $x_2 = 1$, and x_1 changes from 0 to 1, the output $z_1 z_2 = 01$.

(iv) Otherwise, the output is constant.

Turn over

Or

(b) Design an asynchronous circuit that will output only the first pulse received whenever a control input is asserted from Low to High State. Any further pulse will be ignored.

13. (a) (i) Explain in detail about

Delta and Inertial Delay in VHDL.

(ii) What is an Assertion statement ? Explain with suitable example. Also give its severity levels.

Or

(b) Write the VHDL code to realize a decade counter using structural modelling.

14. (a) (i) Explain the I/O block of a Xilinx 4,000 series FPGA. (4 marks)

(b) (ii) Explain PAL 14L4 architecture. (6 marks)

Or

(b) Explain FLEX10K Architecture. (10 marks)

15. (a) (i) Identify the hazard present in the following function :

$$T(x, y, z) = \sum(2, 3, 5, 7).$$

Also derive the hazard-free network.

(5 marks)

(ii) Explain Dynamic Hazard. (5 marks)

Or

(b) For the flow table given, determine all the essential output hazards and essential internal-variable hazards.

	State, output		
x_1, x_2 00	01	11	10
1, 1	2, 0	3, 1	5, 1
4, 0	2, 0	3, 1	8, 1
4, 0	7, 0	3, 1	8, 0
4, 0	6, 1	9, 0	8, 0
4, 0	6, 1	9, 1	5, 1
1, 0	7, 0	9, 1	5, 1

(10 marks)

[4 × 10 = 40 marks]