44800

Name : .....

Reg. No: .....

EIGHTH SEMESTER B.TECH DEGREE EXAMINATION, JUNE 2013
(2004 Scheme)

CS 04 802 – COMPUTER ARCHITECTURE & PARALLEL PROCESSING

Time : Three Hours **Maximum : 100 Marks**

PART –A

I

1. State the role of compilers.
2. How is an instruction set encoded? Give an example.
3. What do you mean by instruction level parallelism?
4. Mention about the compiler and hardware support for instruction level parallelism.
5. How are the cache misses reduced in a system?
6. Differentiate the working of virtual memory and main memory.
7. Define synchronization.
8. Mention the steps involved in connecting more than two computers. (8 x 5 = 40 Marks)

PART –B

II A) Define pipelining. Explain the various hazards in detail.

Or

B) Explain the DLX architecture in detail.

III A) Explain the dynamic scheduling mechanism in detail with an example.

Or

B) Explain the vector processing concept in detail along with its architecture.

IV A) Explain the Unix file system and its performance in detail.

Or

B) Explain the I/O Systems and its working in detail.

V A) Explain the models of memory consistency in detail.

Or

B) With an example, differentiate the working of the centralized memory and the distributed memory architectures. (15 x 4 = 60 Marks)

******