44469

Name : .....

Reg. No: .....

SEVENTH SEMESTER B.TECH DEGREE SUPPLEMENTARY EXAMINATION, JUNE 2013

AI 09 704 – ANALOG AND DIGITAL CIRCUIT DESIGN

Time : Three Hours **Maximum : 70 Marks**

Part A **(5x2=10 Marks)**

1. What is channel length modulation?
2. Give the advantages of folded cascode over simple cascode amplifier.
3. What is slew rate in OP-AMP?
4. Write the entity declaration for a 1-bit half adder in VHDL.
5. Give two examples for Extended Identifiers.

Part B **(4x5=20Marks)**

6. Draw and explain the drain characteristic of MOSFET with varying Vgs.
7. Explain the capacitive model of a MOS device.
8. Explain the operation of a two stage operational amplifier.
9. List the different categories of predefined operators in VHDL.
10. Differentiate between EXIT and NEXT statements.
11. Write a behavioural VHDL program for a 4:1 MUX using if statement.

Part C **(4x10=40 Marks)**

12. (a) i) Derive the equation for threshold voltage of a MOS device.

    ii) Draw and explain cascode current mirror circuit.

    OR

    (b)Derive the gain and frequency response of a Differential Amplifier.

13. (a) Explain the different frequency compensation in Operational Amplifiers.

    OR

    (b)Draw the circuit diagram and explain the operation of a folded cascode amplifier

14. (a) Explain the different types of modelling styles of architecture body in VHDL with examples.

    OR

(b)Describe the different data types in VHDL.

15. (a) Implement structural and behavioural models of a 2:4 decoder in VHDL

OR

(b)Model an up/down counter using structural modelling in VHDL.

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