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Name : .....

Reg. No: .....

SIXTH SEMESTER B.TECH (ENGINEERING) DEGREE EXAMINATION, MAY 2013

EC/PTEC 09 601 – VLSI DESIGN
(2009 Admission)

Time : Three Hours **Maximum Marks**

PART A
Answer all questions

1. What is gradual channel approximation?
2. Draw the static CMOS implementation of a two input NOR gate.
3. Compare Wet etching and Dry etching.
4. What is a stick diagram ?
5. What are LOCOS?

(5 x 2 = 10 Marks)

PART B
Answer any four questions

6. Explain Subthreshold conduction.
7. Explain the factors that contribute for the threshold voltage of a MOSFET.
8. With neat sketch, Explain the function of sense amplifiers in memories.
9. Explain Controllability and Observability.
10. Explain Molecular beam epitaxy.
11. Draw and explain the Layout of a CMOS Inverter.

(4 x 5 = 20 Marks)

PART C
Answer all questions

12. (a) Explain the various second order effects in MOS.

(or)

(b) Explain the operation of a resistive Load nMOS inverter and derive an expression for its (i) V_{OH} (ii) V_{OL} (iii) V_{IL}.

13. (a) With schematic explain the operation of a (i) Carry select adder (ii) Array Multiplier.

(or)

(b) Explain any one test generation method with a suitable example.

14. (a) Discuss in detail about Ion Implantation.

(or)

(b) (i) Discuss the wafer preparation process in context to mechanical and chemical process.
(ii) Why Czochralski (CZ) technique is preferred over other techniques in silicon processing? Explain.

15. (a) (i) Discuss in detail about the metallization process and its types.
(ii) Write a note on Twin Tub process.

(or)

(b) Explain the layout guide lines and draw the layout of a two input NAND gate.

(4 x 10 = 40 Marks)

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