40952

Name : .....

Reg. No: .....

FOURTH SEMESTER B.TECH (ENGINEERING) DEGREE EXAMINATION
APRIL 2013
(2009 Scheme)

EC 09 405 / PT EC 09 404 - COMPUTER ORGANIZATION AND ARCHITECTURE

Time : Three Hours **Maximum : 70 Marks**

PART – A

1. Define effective address.
2. What is a Hardwired control?
3. What is a Cache Memory?
4. Why does DMA have priority over the CPU when both request a memory transfer?
5. What is an interrupt?

(5x 2=10)

PART B

Answer any four questions

6. Give an example for zero address, one-address and three-address instructions.
7. Explain in detail about fixed point arithmetic and floating point arithmetic.
8. Write a note on Random Access Memories.
9. Explain Shared Bus systems.
10. Explain the various registers available in 8085.
11. What are the types of interrupts available in 8085? Explain.

(4x5=20)

PART C

12. (a) Explain the organization of a CPU.

(Or)

(b) Describe the different types of addressing modes in detail.

13. (a) With neat sketch explain the memory organization.

(Or)

(b) Discuss the various mapping schemes used in cache design. Compare them.

14. (a) With neat diagram explain how DMA transfer is accomplished.

(Or)

(b) Explain the functions to be performed by I/O interface.

15. (a) With block diagram explain 8085 architecture.

(Or)

(b) Discuss in detail about Memory mapped I/O and I/O mapped I/O.

(4 x 10 =40)

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