C 40948
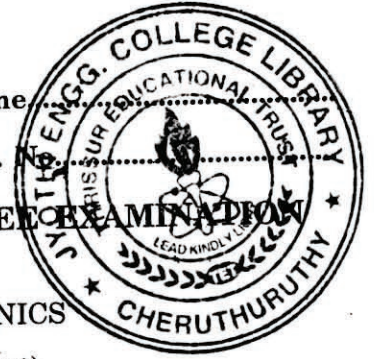
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FOURTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION APRIL 2013

EE 09 405/PT EE 09 404—DIGITAL ELECTRONICS

(2009 Scheme—Regular/Supplementary/Improvement)

Time : Three Hours

Maximum : 70 Marks

Part A

1. Define Noise Margin.

2. Draw the symbol of tristate buffer and define its operation.

3. Convert the following :

    (a) $(1101.101)_2$ = (   )$_{16}$.

    (b) $(367)_8$ = (   )$_2$.

4. Differentiate between Decoder and Demultiplexer.

5. What are the applications of Johnson counter ?

(5 × 2 = 10 marks)

Part B

6. Explain current sourcing and sinking action in TTL.

7. Draw the simplified logic circuit for the given Boolean expression.

$$Y = \overline{X}\overline{Y}\overline{Z} + \overline{X}\overline{Y}Z + X\overline{Y}Z + XYZ.$$

8. With example, show how 8 × 1 Multiplexer is used for implementing four variable functions.

9. Define and state difference between RAM, ROM and EPROM memories.

10. List the various components of Arithmetic and logic unit and state the function of each.

11. What is the difference between std-logic vector and bit vector in VHDL ? Explain with example.

(4 × 5 = 20 marks)

Part C

12. (a) Discuss in detail the various characteristics of TTL IC.

Or

    (b) Explain the CMOS transmission gate and its features.

Turn over

13. (a) Draw the schematic of BCD adder and explain how it can be used with an example.

Or

(b) Describe the operation a Multiplexer and show how a 16 input multiplexer is used to generate the function.

$$Z = \overline{A}\overline{B}\overline{C}D + BCD + A\overline{B}\overline{D} + AB\overline{C}D.$$

14. (a) Draw and explain a MOD-8 synchronous up/down counter.

Or

(b) Discuss the ROM architecture along with timing diagram.

15. (a) Write the VHDL code for a 4 bit parallel adder with Full Adder as the basic element.

Or

(b) Discuss the architecture of 8085 microprocessor.

(4 × 10 = 40 marks)