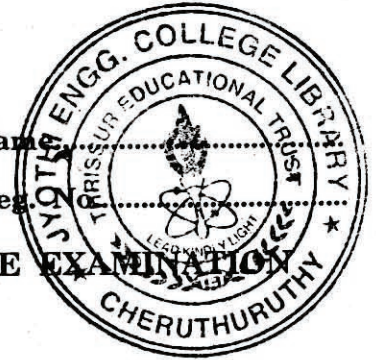


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Name

Reg.



**SIXTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION
MAY 2013**

CS/PTCS 09 601—EMBEDDED SYSTEM

(2009 Admission onwards)

Time : Three Hours

Maximum : 70 Marks

Part A

Answer all questions.

1. Mention about the design metrics of an embedded system.
2. Write about the advantages of using pipelining.
3. Write about the cache impact on system performance.
4. Write about the models vs. languages.
5. What do you mean by logic synthesis ?

(5 × 2 = 10 marks)

Part B

Answer any four questions.

6. Explain about the working of Timers and Counters.
7. Explain about the compilation / synthesis mechanism in IC technology.
8. Explain about the memory management unit.
9. Write about the principle of operation involved in wireless communication.
10. Explain about the features of QNX.
11. Explain about FSM synthesis.

(4 × 5 = 20 marks)

Part C

12. (a) Explain about the instruction set, program and data memory space of VLIW architecture.

Or

- (b) Explain in detail about the custom single purpose processor design and optimization.

13. (a) Explain in detail about the cache mapping techniques.

Or

- (b) Explain about Microprocessor interfacing in detail.

Turn over

14. (a) Explain in detail about the program state machine model (PSM).

Or

(b) Explain about the interprocess communication mechanism.

15. (a) Explain about the two-level and multi-level logic minimization.

Or

(b) Write in detail about the intellectual property cores.

(4 × 10 = 40 marks)