C 41638

Name.....

Reg. No.....

EIGHTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, APRIL 2013

CS 09 801—COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

(2009 Admissions)

Time : Three Hours Maximum : 70 Marks

Part A

1. How to evaluate CPI ?
2. List out the possible data hazards.
3. Explain total store ordering.
4. What is meant by memory access time ?
5. How many bits are in the (0, 2) branch predictor with 4K entries ?

(5 × 2 = 10 marks)

Part B

6. Explain the qualitative principles of computer design.
7. List out the limitations on instruction level parallelism for realizable processors.
8. What are the basic cache optimizations ? Explain the benefits.
9. With a neat diagram, explain shared memory.
10. Explain little queuing theory.
11. Explain pipeline scheduling and loop unrolling with proper example.

(4 × 5 = 20 marks)

Part C

12. (a) Explain addressing modes with simple example codes in detail.

Or

(b) What is a pipeline hazard ? Explain various types of hazards in detail.

13. (a) With a neat diagram, explain the basic structure of a MIPS floating-point unit using Tomasulo's algorithm.

Or

(b) Explain the various steps for enhancing vector performance.

14. (a) With a neat diagram explain virtual memory and its protection.

Or

(b) What is the use of bench-mark ? Explain various types of bench-marks in detail.

15. (a) With a neat diagram, explain cache coherence in a distributed shared memory multiprocessor.

Or

(b) Explain compiler optimization and consistency model in detail.

(4 × 10 = 40 marks)