41264 B

Name : .....

Reg. No: .....

SIXTH SEMESTER B.TECH (ENGINEERING) DEGREE EXAMINATION,
MAY 2013
(2009 Admissions)

AI 09 L03 – DIGITAL DESIGN WITH VHDL

Time : Three Hours **Maximum : 70 Marks**

PART A
(Answer all questions)

1. What are the assignment operators in VHDL
2. Differentiate between bit and std_logic
3. What is the relevance of entity part in a VHDL Design
4. What is a port ?
5. Give an example for user defined attribute 5 x 2 = 10

PART B
(Answer any 4 questions)

6. What do you meant by Subtype? List a few advantages of having Subtype instead of defining a new data type
7. Design a 4 bit grey to binary code converter in VHDL
8. Give the differences between STD_LOGIC and STD_U LOGIC
9. What are the different signal attributes in VHDL
10. What are the different ways of Port mapping ? Elaborate with examples
11. Write a test bench for a half adder circuit (The input vectors are to be read from infile1.txt) 4 x 5 = 20

PART C
(Answer all questions)

12 A) Obtain the VHDL model for a 1 to 8 DEMUX

Or

B) What are the different pre defined operators in VHDL give examples

13 A) Design an n bit Generic ripple adder using VHDL

Or

Turn over

B) Write notes on i) operator overloading ii) signal attributes

14 A) Design a 4 bit carry look ahead adder with a carry look ahead unit as a component

Or

B) Design an ALU unit in VHDL with Components declared in a package

(Assume the logic unit can perform AND, OR ,NAND,NOR ,XOR,XNOR ,NOT operations and Arithmetic unit can perform ADD, SUB, Increment , Decrement , Multiply , Divide) (State assumptions clearly)

15 A) Explain briefly the various methods adopted in testing digital circuits

Or

B) Write a test bench for a full subtractor circuit (The input vectors are to be read from a infile1.txt and output is stored in outfile1.txt)

4 x 10 = 40

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