D 30966 (Pages : 2) Name.....

Reg. No.....

FIFTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION OCTOBER 2012

EE 09 505—DIGITAL SYSTEM DESIGN

(2009 Scheme)

Time : Three Hours Maximum : 70 Marks

Part A

1. List the STD_LOGIC values in VHDL.
2. Write the VHDL code to produce the following output functions :

   $X = A + B$

   $Y = AB$.
3. What is meant by 'Bubble-to-Bubble' logic design ?
4. Differentiate between Moore machine and Mealy machine.
5. Differentiate between PLDs and CPLDs. Give one example.

(5 × 2 = 10 marks)

Part B

Answer any **four** *out of six.*

1. List the essential features of VHDL language.
2. What is a test bench ? Give one simple example.
3. Differentiate between functions and procedures in VHDL.
4. Write a brief note on bi-state devices.
5. What are pipelined outputs ?
6. What do you understand by race free state assignment ?

(4 × 5 = 20 marks)

Part C

1. Discuss the features of libraries and packages in VHDL with example.
2. What are the various ways in which types, constants and arrays are defined in VHDL ?
3. (a) Explain bubble-to-bubble logic design. (4 marks)

   (b) Write the VHDL code for a 2 to 4 decoder in all 3 styles of modelling. (6 marks)

Or

4. Write the VHDL code to realize a 4 bit magnitude comparator.

Turn over

5. Design a sequential circuit with two DFFs A and B, and one input x when $x = 0$, the state of the circuit remains the same. When $x = 1$, the circuit goes through the state transition from 00 to 01 to 11 to 10 back to 00 and repeats.

Or

6. Write the VHDL description of 4 bit up-down-counter with parallel load using following control inputs.

   (a) Has 3 control i/ps for 3 operations up, down and Load. The order of precedence is Load, Up and Down.

   (b) The counter has 2 selection i/ps to specify four operations : Up, Down, Load and no-change.

7. Find a hazard-free implementation of the function :

$$f(x_1, \ldots, x_4) = \Sigma m(0,4,11,13,15) + D(2,3,5,10)$$

Or

8. Discuss the features of 9500 CPLD family.

[4 × 10 = 40 marks]