D 30906 (Pages : 2) Name.....

Reg. No.....

THIRD SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION
OCTOBER 2012

Electronics and Communication Engineering

EC 09 305/PTEC 09 304—DIGITAL ELECTRONICS

(2009 Admissions)

Time : Three Hours Maximum : 70 Marks

Part A

Answer **all** *questions.*

1. Simplify the Boolean function $F(w, x, y, z) = \sum(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$.
2. What are universal gates ?
3. Perform 1010100 – 1000011 using 1's and 2's complements.
4. Draw the JK flip-flop with truth table.
5. Write the difference between sequential circuits and combinational circuits.

(5 × 2 = 10 marks)

Part B

Answer any **four** *questions.*

6. Simplify in sum of products and product of sums

$$A\bar{C} + \bar{B}D + \bar{A}CD + ABCD.$$

7. Draw a NAND logic diagram that implements $F(A, B, C, D) = \sum(0, 4, 12)$.
8. Implement $F(A, B, C) = \sum(1, 2, 4, 5)$ with a multiplexer.
9. Give the excitation tables of JK, SR and T flipflops.
10. What is ring counter ?
11. Write the importance of ASM chart with example.

(4 × 5 = 20 marks)

Turn over

Part C

Answer section (a) **or** *section* (b) *of each question.*

12. (a) Simplify the Boolean function $F(A, B, C, D, E) = \sum(0, 2, 4, 6, 9, 13, 21, 23, 25, 29, 31)$ and implement using minimum number of NOR gates.

Or

(b) Explain Quine Mc Cluskey method with an example.

13. (a) Draw the logic diagrams of a look ahead carry generator and 4-bit full adder with look ahead carry and explain the operations.

Or

(b) Explain the working of (i) TTL NAND gate and (ii) ECL gate with neat diagrams.

14. (a) (i) Construct a Mod-10 counter. (5 marks)

(ii) Construct a 4-bit up-down counter. (5 marks)

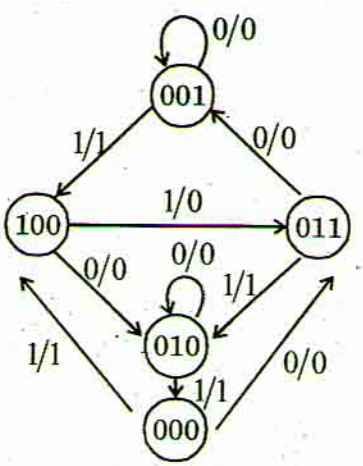
Or

(b) Explain the working principle of universal shift register with neat diagrams. (10 marks)

15. (a) A sequential circuit has three flip-flops A, B, C ; one input x and one output y. The state diagram is given in Fig (1). The circuit is to be designed by treating the unused states as don't care conditions.

(i) Use D flip-flops in the design.

(ii) Use JK flip-flops in the design.



Or

(b) Design a counter with the following repeated binary sequence using T flip-flops.

(i) 0, 1, 2, 3, 5, 6.

(ii) 0, 1, 3, 7, 6, 4.

(4 × 10 = 40 marks)