C 29714 (Pages : 2) Name.....

Reg. No.....



# SEVENTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION
# OCTOBER 2012

## EC 09 704—DIGITAL SYSTEM DESIGN

(2009 admissions)

Time : Three Hours Maximum : 70 Marks

## Part A

*Answer* **all** *questions.*

1. What is an asynchronous sequential circuit ?
2. What are the two basic rules for state assignment ?
3. State the difference between Delta delay and Inertial delay in VHDL.
4. State the difference between PAL and PLA.
5. What is an Hazard ?

(5 × 2 = 10 marks)

## Part B

*Answer any* **four** *questions.*

6. Explain the cycles and races with a suitable example.
7. What is an incompletely specified state machine ? Give an example.
8. Write the VHDL code for a D flip flop using behavioural modeling.
9. Draw the structure of the output portion of PAL 14L4 and PAL 12H6 and explain the difference.
10. Explain static hazard and its avoidance using K-Map.
11. Explain clock skew.

(4 × 5 = 20 marks)

## Part C

*Answer* **all** *questions.*

12. (a) Explain the fundamental mode and pulsed mode asynchronous sequential circuits using suitable examples.

*Or*

(b) Explain the state minimization using partitioning procedure.

13. (a) (i) Write the VHDI code for a full adder using structural modeling and explain the code.

(ii) What is an attribute ? Explain.

*Or*

(b) Design a 3-bit parallel in serial out shift register and write the VHDL code using structural modeling.

Turn over

14. (a) With block diagram explain the 22V10 architecture.

*Or*

(b) Explain the architecture of XC 9500 family devices.

15. (a) Explain in detail about Dynamic Hazard and Essential Hazards.

*Or*

(b) (i) Explain in detail about synchronization and its failure.

(ii) Explain the Metastability behaviour of flip flops.

(4 × 10 = 40 marks)