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Name:

Reg. No.

SEVENTH SEMESTER B.TECH. DEGREE EXAMINATION,
OCTOBER 2012
EC.09.703 - ANALOG AND MIXED MOS CIRCUITS

Time: Three hours

Maximum : 70 marks

PART – A (5 X 2 = 10 MARKS)

1. What is Latch up?
2. Draw the schematic of a simple MOS current mirror.
3. Define Gain and Bandwidth of an Amplifier.
4. What is the significance of a switched capacitor circuits?
5. What is a loop filter?

PART – B (4 X 5 = 20 MARKS)

ANSWER ANY FOUR QUESTIONS

6. Explain the limitations of CMOS technology?
7. Derive an expression for the R_{out} of a simple current mirror.
8. With circuit schematic explain single stage amplifier.
9. With schematic, explain the operation of a switched capacitor integrator and derive its output expression.
10. Explain the operation of a fully differential first-order switched capacitor filter.
11. Explain the operation and application of a sample and hold circuit.

PART – C (4 X 10 = 40 MARKS)

12. (a) Briefly explain the low frequency model parameters and derive them for an n-channel transistor that has doping concentrations of $N_D = 10^{25}$, $N_A = 10^{22}$, $\mu_n C_{ox} = 22 \mu A/V^2$, $W/L = 20 \mu m/2 \mu m$, $V_{GS} = 1.2 V$, $V_{tn} = 0.8 V$ and $V_{DS} = V_{eff}$. Assume $\gamma = 0.5(V)^{1/2}$ and $V_{SB} = 0.5 V$. What is the new value of r_{ds} if the drain source voltage is increased by 0.5 V?

(or)

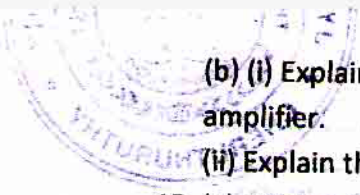
- (b) Explain the operation of MOSFET as a Switch and active resistor. What is charge feed through effect ? How it is avoided?

13. (a) With circuit schematic explain the operation of a CMOS differential amplifier with current mirror load.

(or)

- (b) Derive the small signal model of a simple cascade amplifier and derive its frequency response.

14. (a) Explain the design procedure of two stage operationa amplifier.



(or)

(b) (i) Explain the influence of clock feedthrough on a non-inverting switched capacitor amplifier. (5)

(ii) Explain the miller compensation in two stage operational amplifiers. (5)

15. (a) Discuss in detail about the operation and application of a PLL.

(or)

(b) Explain the operation of a Gilbert Cell and configure it as a Four quadrant multiplier.