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Name.....

Reg. No.....

FOURTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, FEBRUARY 2013

EC 04 404 – COMPUTER ORGANIZATION AND ARCHITECTURE

(2004 Admissions)

Time : Three Hours Maximum : 100 Marks

Answer **all** *questions.*

1. (a) Draw and explain the flowchart of an iterative design process of a system.

   (b) Explain the user and supervisor modes of programs executed by a general purpose computer.

   (c) Write the non-restoring division algorithm for unsigned integers.

   (d) What are the two systematic approaches to the design of hardwired controllers. Write the steps of any *one* design method.

   (e) Write down the conceptual organization of a multilevel memory system in a computer.

   (f) Draw the logic circuit of an associate memory cell and explain its working.

   (g) Compare the various interconnection structures of computers.

   (h) Explain the process of bus arbitration using daisy chaining.

   (8 × 5 = 40 marks)

2. (a) Explain how fixed-point multiplication is implemented in computers. Illustrate the process of multiplication using a suitable example.

   Or

   (b) Explain with a block diagram the organization of a CPU with its registers.

3. (a) Explain with a block diagram the working of a carry-look ahead adder.

   Or

   (b) Discuss the general structure and behaviour of control units.

4. (a) List the physical differences between the following memory technologies :

   SRAMS, Flash memories, Magnetic floppy disks, Optical hard disks, and CD-ROMs.

   Or

   (b) Design a direct-mapped cache with the following parameters : the capacity of the cache is to be reduced to 64 kB, and the cache block size and the width of the system data bus are both to be 32 bits.

5. (a) Explain the use of Tristate logic for bus interfacing.

   Or

   (b) Explain the vectored interrupt scheme and interrupt handlers location in memory.

   (4 × 15 = 60 marks)