D 30911 (Pages : 2) Name.....

Reg. No.....

THIRD SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION
OCTOBER 2012

IT /CS 09 306 / PTCS 09 305—SWITCHING THEORY AND LOGIC DESIGN

Time : Three Hours Maximum : 70 Marks

Part A

Answer **all** *questions.*

1. Convert the binary number 1101. 0110111 to octal number.
2. Draw the logic diagram for exclusive NOR gate.
3. Define Prime cube theorem.
4. What is meant by fault tolerance ?
5. Give *two* applications for shift registers.

(5 × 2 = 10 marks)

Part B

Answer any **four** *questions.*

6. Convert the following expressions to sum-of-product forms :

$$(A+C)(ABC+ACD) \text{ and } \left(A+\overline{B}C\right)D.$$

7. Implement the following using NAND gates :

$$\overline{A}\left[B+\overline{C}(D+E)\right] \text{ and } \left(\overline{A}\,\overline{B}+\overline{CD}\right).$$

8. Write notes on Read Only Memory.
9. Explain PLA folding.
10. Illustrate the procedure for designing sequential circuits.
11. Write notes on state tables and diagrams.

(4 × 5 = 20 marks)

Part C

Answer **all** *questions.*

12. (a) Apply DeMorgan's theorems to the following :

$$\overline{\overline{AB}\left(CD+\overline{E}F\right)\left(\overline{AB}+\overline{CD}\right)} \text{ and } \overline{\left(A+\overline{B}+C+\overline{D}\right)}+\overline{ABC\overline{D}}$$

Or

Turn over

(b) Explain the simplification using Quine-McClusky method.

13. (a) Describe the working of a multiplexer with suitable logic diagram and truth table.

Or

(b) Explain the operation of two-digit BCD-to-binary converter using full-adders.

14. (a) Write notes on PLA minimization.

Or

(b) Write notes on fault classes and fault models.

15. (a) Illustrate the operation of 4-bit parallel- in parallel-out shift registers.

Or

(b) Explain the operation of a three bit synchronous counter with its timing diagram.

(4 × 10 = 40 marks)