(Pages: 2)

THIRD SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION DECEMBER 2012

CS/ IT 04 305 —SWITCHING THEORY AND LOGIC DESIGNATION

(2004 Admissions)

Time: Three Hours

Maximum: 100 Marks

Answer all questions.

Part A

I. (a) Convert the following number conversion:

(i)
$$(2BC)_{16} = (?)_{10}$$

(ii)
$$(7300)_{10} = (?)_{16}$$

(iii)
$$(1000)_{10} = (?)_8$$

(b) Prove that following theorems:

(i)
$$\overline{A}B\overline{C} + \overline{A}BC + \overline{A}\overline{B}C = \overline{A}\overline{B} + \overline{A}C$$
.

(ii)
$$AB + BC + CA = (A + B)(B + C)(C + A)$$
.

- (c) Design a full adder circuit.
- (d) Draw and explain 3 to 8 decoder circuit.
- (e) Explain about fault model.
- (f) Explain what is meant by path sensitizing.
- (g) Explain what is meant by race around condition.
- (h) What is meant by ripple counter? Explain.

 $(8 \times 5 = 40 \text{ marks})$

Part B

II. (a) Reduce the following functions by Karnaugh map and represent the reduced function in sum of products and product of sums forms:

$$F = \pi (0, 1, 2, 3, 8, 9, 10, 11, 14, 15, 20, 21, 22, 23, 24, 25)$$

(b) Using Quine-McClusky method reduce the following function:

$$Y = \sum (0, 2, 3, 10, 11, 12, 13, 16, 17, 18, 19, 20, 21, 26, 27).$$

III. (a) Design a logic circuit to convert 2-4-2-1 code to 8-4-2-1 code.

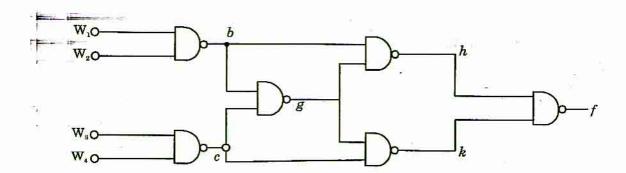
Or

- (b) Design a combinational circuit using a ROM. The circuit accepts a 3-bit number and generates an output binary number equal to the square of the input number.
- IV. (a) Devise a test to distinguish between two circuits that implement the following expressions:

$$f = x_1 x_2 x_3 + x_2 \overline{x}_3 x_4 + \overline{x}_1 \overline{x}_2 x_4 + \overline{x}_1 x_3 \overline{x}_4$$
$$g = (\overline{x}_1 + x_2)(x_3 + x_4).$$

Or

(b) List all single faults in the circuit shown below that can be detected using each of the tests $W_1 \ W_2 \ W_3 \ W_4 = 1100,0010,$ and 0110.



- V. (a) With neat diagrams, explain the working of
 - (i) Serial-in, serial out
 - (ii) Parallel- in, serial out

shift registers.

Or

(b) Design a sequential circuit to count the following sequence repeatedly using J-K-flip-flop:

1, 3, 7, 0, 1, 3, 7, 0,

 $(4 \times 15 = 60 \text{ marks})$