32981

Name : .....

Reg. No: .....

THIRD SEMESTER B.TECH (OLD SCHEME) DEGREE EXAMINATION, FEBRUARY 2013

AI/BM 04 305 - DIGITAL SYSTEMS

Time: 3 hours **Maximum: 100 marks**

I. (a) State and prove absorption theorem.

(b) Perform the subtraction using 1's complement and 2's complement arithmetic 35_{10}-56_{10}

(c) Design a Half Adder adder.

(d) Explain the structure of a PROM and PLA.

(e) What is a Multivibrator? Explain.

(f) Explain Totem Pole and Open Collector outputs.

(g) Briefly explain the difference between Mealy Machine and Moore Machine.

(h) What are incompletely specified State Machines? Give example.

(8 x 5 = 40 Marks)

II. (a) (i) State and Prove De Morgan's theorem.

(ii) Give the canonical form of the following function

F(A,B,C,D)= A'B+B'C+C'D+A'D

(Or)

(b) Simplify the following function using (i) K-Map (ii) Quin Mc Cluskey method

F(A,B,C,D) = ∑m(1,3,4,5,6,7,8,9,12,15)

III. (a) Design and explain the operation of a BCD Adder.

(Or)

(b) (i) What is race around condition? How it is avoided using Master Slave configuration?

(ii) Implement the following function using suitable multiplexer

F(A,B,C,D) = ∑m(1,2, 5,6,9,10)

IV. (a) With logic diagram explain the operation of a Universal Shift register.

(Or)

(b) (i) Design a Mod 5 counter.

(ii) With schematic explain the operation of a two input TTL NAND gate.

V. (a) With a suitable example explain partitioning procedure for state minimization.

(Or)

(b) Explain Pulse Mode and Fundamental mode asynchronous sequential circuits with examples.

(4 x 15 = 60 Marks)

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