D 30914 (Pages : 2) Name.....

Reg. No.....



# THIRD SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION OCTOBER 2012

Applied Electronics and Instrumentation

AI 09 305—DIGITAL SYSTEMS

Time : Three Hours Maximum : 70 Marks

## Part A

*Answer* all *questions.*

1. Convert $22.20_{10}$ to its binary equivalent.
2. Compare 1's complement and 2's complement form.
3. Design a Half Adder.
4. Covert JK flip flop into a D flip flop.
5. What is a totem pole output ?

(5 × 2 = 10 marks)

## Part B

6. Write a note on Error detecting Codes.
7. State and prove De Morgan's theorem.
8. Simplify $F = (A + \overline{B} + \overline{C})(A + \overline{B} + C)$.
9. Design a Binary-Gray decoder.
10. How frequency division is achieved using flip flops ? Give the general expression for it.
11. State the condition for state equivalence. Give an example.

(4 × 5 = 20 marks)

## Part C

12. (a) Explain any one Error detecting and Correcting code.

*Or*

(b) Determine the prime implicants of the function.

$$F(A, B, C, D) = \Sigma(0, 1, 2, 3, 5, 6, 7, 8, 11, 13).$$

13. (a) Design an octal to binary encoder.

*Or*

(b) Discuss in detail about :

(i) Static RAM.

(ii) Dynamic RAM.

Turn over

14. (a) Design a 3-bit bidirectional shift register.

*Or*

(b) Explain the features of :

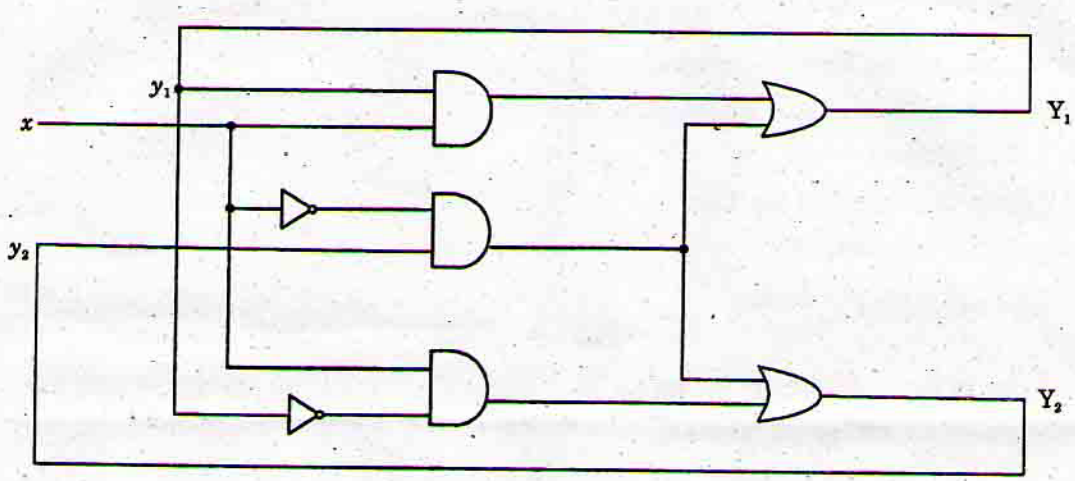
(i) TTL.

(ii) ECL.

(iii) CMOS.

logics.

15. (a) Obtain the transition table and flow table for the given asynchronous sequential circuit.




*Or*

(b) Design a serial parity generator using the asynchronous FSM technique.

(4 × 10 = 40 marks)