29763

Name :.....

Reg. No :.....

SEVENTH SEMESTER B.TECH DEGREE EXAMINATION, OCTOBER 2012

AI 09 704 - ANALOG AND DIGITAL CIRCUIT DESIGN

Time : Three Hours **Maximum : 70 Marks**

PART A (5 x 2=10 Marks)

1. What is body effect?
2. State the difference between current source and current mirror.
3. What is charge feedthrough?
4. What are the primary design units in VHDL?
5. Write the architecture body for a tristate buffer using behavioral modeling.

PART B (4 x 5 = 20 Marks)

Answer any four questions.

6. Briefly explain the Cascode current mirror and its advantages.
7. Explain the frequency compensation in Operational Amplifiers.
8. Draw the schematic of a Switched capacitor integrator and explain its operation.
9. Briefly explain the various classes of Data types in VHDL.
10. Explain the generate and generic statements in VHDL with suitable examples.
11. Implement the following expression using a suitable PLA
    $F(A,B,C) = \sum m(0,2,3,5,7)$

PART C (4x 10 = 40 Marks)

All questions carry equal marks

12. (a) With neat sketch explain the MOS device structure.

    (or)

    (b) Derive the gain and frequency response of a Differential amplifier.

13. (a) With circuit schematic explain the operation of folded cascode amplifier.

    (or)

    (b) (i) With schematic explain the operation of a summing amplifier and derive an expression for its output.

    (ii) Explain the operation of a two stage operational amplifier.

14. (a) Write the VHDL code for a Full Adder using (i) Data Flow and (ii) Structural Modeling.

    (or)

    (b) With suitable examples, explain the Assertion and Report statements with their default severity levels.

15. (a) Write the VHDL code for a 8x1 Multiplexer using select and case statements in VHDL.

    (or)

    (b) Write the VHDL code for a 4x4 array multiplier using structural modeling in VHDL.

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