26773

Name : .....

Reg. No: .....

SIXTH SEMESTER BTECH DEGREE EXAMINATION

AIO9 601 - DIGITAL SIGNAL PROCESSING
(2009 Admission)

Time : 3 Hours Maximum : 70 Marks

PART A

(Answer All Questions)

1. Show that DFT is a linear transform.
2. State the convolution property of the DFT.
3. Name any two errors that occur due to finite word length effects in DSP's.
4. Define linear phase characteristics of a filter.
5. What is a MAC in s DSP chip? (5 x 2 = 10 Marks)

PART B

(Answer any 4 questions)

6. Show that DFT of real signal is conjugate symmetric and DFT of a conjugate symmetric signal is real.
7. A data sequence having 10,000 samples is to be filtered using a 101 FIR filter. The filter is implemented in the DFT domain using 512 point DFT and overlap add method. Find out the perceritage savings in computation (number of multiplications and additions required) compared to the direct implementation of convolution.
8. Draw the signal flow graph of direct form realizations (Type I and Type II) for the IIR filter represented by

$$\frac{1+2z^{-1}+3z^{-2}+2z^{-3}}{1+0.9z^{-1}-0.8z^{-2}+0.5z^{-3}}.$$

9. Using bilinear transform, determine the digital filter transfer function corresponding to the analog filter.
10. Discuss the architecture design enabling parallel processing in a Digital Signal Processor.

$$H(s)=\frac{8+0.1}{(8+0.1)^2+9}.$$ Take T = 1. (4 x 5 Marks = 20 Marks)

PART C

(Answer any one question from each Module)

MODULE I

11. (a) Show that linear convolution can be implemented through circular convolution and describe the steps involved in implementing linear filtering in the DFT domain using overlap save method.

    (b) With appropriate signal flow graph, explain the implementation of decimation in time FFT algorithm for computing an 8 point DFT. Also determine the number of complex multiplications and additions required for the DFT computation.

MODULE II

12. (a) Draw the direct form realization and lattice structure realization of the FIR filter represented by the transfer function $H(z) = 1 + 2.88z^{-1} + 3.404z^{-2} + 1.74z^{-3} + 0.4z^{-4}$.

    (b) Obtain the impulse response of the filter y(n) = x(n)+0.5y (n-1) assuming 4 bit representation for the coefficients and input x(n).

MODULE III

13. (a) Determine the system function H(z) of the lowest-order Chebyshev digital filter that meets the following specifications.

    (i) 0.5 dB ripple in the pass-band $0 \le |w| \le 0.24\pi$

    (ii) At least 50 dB attenuation in the stop-band $0.35\pi \le |w| \le \pi$. Draw the Direct form II implementation of the filter.

    (b) Design an FIR linear phase filter using frequency sampling method approximating the ideal frequency response.

$$H(w) = \begin{cases} 1, \ for \ |w| \le \frac{\pi}{6}, \\ 0, \ for \ \frac{\pi}{6} < |w| \le \pi \end{cases}$$

Assume filter length L = 11. Draw the filter structure in Direct form.

MODULE IV

14. (a) What are the distinct features of DSP processor architecture? Explain with an example processor architecture.

    (b) What is meant by instruction pipelining? Explain with an example how pipelining increases through put efficiency.

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