28984

Name : .....

Reg. No: .....

SEVENTH SEMESTER B.TECH DEGREE EXAMINATION, JUNE 2012

AI 04 703 DIGITAL MOS CIRCUITS

Time : Three Hours **Maximum : 100 Marks**

I. (a) Explain subthreshold channel conduction current.

(b) State and explain body effect.

(c) How to calculate the delay times in CMOS inverters? Explain.

(d) What is a Super Buffer? Explain with its schematic.

(e) Write a note on AOI and IOA gates.

(f) Explain the features and advantages of BiCMOS.

(g) What is charge sharing? Explain.

(h) What is an adiabatic logic? Explain.

(8 x 5 = 40 Marks)

2. (a) (i) Explain the short channel effects.

(ii) Write a note on Voltage scaling.

(or)

(b) With neat sketch explain the MOSFET model in detail.

3. (a) (i) With schematic Explain the operation of a CMOS inverter.

(ii) What is a Pseudo NMOS logic style? Why it suffers static power dissipation?

(or)

(b) Derive an expression of the V_{IL} and V_{OH} of a CMOS inverters.

4. (a) (i) With schematic Explain the operation of a CMOS NAND

(ii) What is Boot Strapping ? Explain

(or)

(b) (i) Explain the operation of a Transmission gates.

(ii) Draw the schematic of a 4x1 Multiplexer using Pass Transistor Logic.

5. (a) Discuss in detail about the Precharge and Evaluation phase of a Dynamic CMOS logic.

(or)

(b) Explain in detail about (i) NORA logic (ii) True Single Phase clock dynamic logic.

(4 x 15 = 60 Marks)

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