D 23533 (Pages : 2) Name.....

Reg. No.....

THIRD SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION DECEMBER 2011

AI/BM 04 305—DIGITAL SYSTEMS

Time : Three Hours Maximum : 100 Marks

Answer **all** *questions.*

Part A

I. (a) Convert 11110000_2 in a signed 2's complement system to a decimal number.

(b) What do you understand by the terms :

(i) min-terms ;

(ii) max-terms ?

Explain.

(c) Draw the circuit diagram for decimal to BCD encoder and explain.

(d) Draw and explain the operation of SR flip-flop using NAND gates.

(e) Draw the circuit of mod-5 counter and explain.

(f) List the characteristics of digital IC families.

(g) Distinguish between Asynchronous and Synchronous sequential circuits.

(h) Explain the term : Finite state model.

($8 \times 5 = 40$ marks)

Part B

II. (a) (i) Convert the following :

(1) $0.12_{10} = (?)_{16}$.

(2) $(2096)_{10} = (?)_{16}$.

(4 marks)

(ii) Simplify the Boolean expression :

$$F = \overline{(\bar{A}C+B\bar{C})(A+\bar{B}+D)}.$$

(5 marks)

(iii) Explain why NAND and NOR are called universal gates. (6 marks)

Or

(b) Reduce the following function using Quine McClusky method and realize the reduced expression using logic gates.

$F(A, B, C, D, E) = \Sigma (0, 1, 4, 5, 16, 17, 21, 25, 29)$.

Turn over

III. (a) (i) Draw and explain full adder with truth table. (8 marks)

(ii) Explain the basic structure of RAM. (7 marks)

Or

(b) (i) Explain how a J.K. flip-flop can be constructed using a clocked SR flip-flop. (6 marks)

(ii) Draw 1 of 16 demultiplexer using NAND gates and explain. (9 marks)

IV. (a) Design a sequential circuit for displaying the following sequence :

0, 1, 3, 7, 0, 1, . . .

Or

(b) (i) Draw the circuit of TTL NAND gate and explain. (8 marks)

(ii) Write short note on BiCMOS circuit. (7 marks)

V. (a) Design a 2-input and 2-output synchronous sequential circuit which produces an output Y = 1, whenever any of the following input sequences occurs :

1101, 1011, 1001.

The circuit resets to the initial state after a 1 output is generated.

Or

(b) Draw the state diagram and the state table for a 4-bit odd-parity generator.

(4 × 15 = 60 marks)