Name...

Reg. No

FIFTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION DECEMBER 2011

AI/BM 04 503—ADVANCED MICROPROCESSORS AND MICROCONTROLLERS

(2004 Admissions)

Time: Three Hours

Maximum: 100 Marks

Part A

Answer all the questions. Each question carries 4 marks.

- 1. (a) Write a note on any two program development tools.
 - (b) Explain the bus structure of 8086 processor.
 - (c) List the salient features of 80386 microprocessor.
 - (d) What is meant by super scalar architecture? What are its advantages?
 - (e) Explain the auto reload timer mode of 8051.
 - (f) Write a note on register banks of 8051.
 - (g) Explain the instruction MOVC A, @ A+DPTR. Identify the type of addressing.
 - (h) Draw the interrupt structure of 8051.

 $(8 \times 5 = 40 \text{ marks})$

2. (a) Discuss the various signals that are common to both modes and specific to each mode in 8086.

· Or

(b) Explain the 8086 multiprocessor configuration.

(15 marks)

3. (a) Draw the Internal architecture of pentium processor and explain.

Or

- (b) (i) Describe about 80386 descriptor.
 - (ii) Distinguish between real, protected and virtual modes of 80386.

(15 marks)

4. (a) (i) Discuss the Read-Modify-Write feature of 8051 port.

(7 marks)

(ii) Discuss the hardware method of controlling the start and stop of timer.

(8 marks)

Or

(b) Draw the internal RAM and ROM organisation of 8051 and explain.

(15 marks)

Turn over

- 5. (a) (i) Write an 8051 ALP to generate a square wave of 5 kHz frequency at pin P 1.5 of 8051 controller. (6 marks)
 - (ii) Explain the interfacing of DAC with 8051.

(9 marks)

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(b) How does controller differentiate between timer and counter operation? Explain with suitable diagrams. (15 marks)

Each queition carries 4 marks

What is meant by super scalar architecture? What are its advantages?

Draw the Internal architecture of pentium processor and explain.

(a) Discuss the hardware method of controlling the start and stop of times

4. (a) (i) Discuss the Read-Modify-Write Senture of 8051 fort.

 $[4 \times 15 = 60 \text{ marks}]$

(h) Draw the interrupt structure of 2051