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Name : .....

Reg. No: .....

EIGHTH SEMESTER B.TECH (ENGINEERING) DEGREE EXAMINATION, MAY 2012

CS 04 802 – COMPUTER ARCHITECTURE AND PARALLEL PROCESSING
(2004 Admissions)

Time : Three Hours **Maximum : 100 Marks**

PART – A

I (a) Define pipelining. Explain its working.

(b) Write a note on the quantitative principles of computer design.

(c) Explain about the enhancing vector performance mechanism

(d) Write in detail about the hardware support for the instruction level parallelism.

(e) How is protection done in the Intel Pentium Processor?

(f) Write about the reliability and availability mechanism.

(g) Discuss about the practical issues involved in connecting more than two computers.

(h) Explain the models of memory consistency.

$(8 \times 5 = 40)$

PART – B

II (a) Explain in detail about the pipelining mechanism.

(Or)

(b) Write a note on
(i) Role of compilers in a computer system.
(ii) Encoding an instruction set

III (a) Explain in detail about the dynamic scheduling and the dynamic hardware prediction methodology.

(Or)

(b) Discuss in detail about the vector architecture. Compiler vectorization and the vector length.

IV (a) Explain in detail about the working of virtual memory with examples.

(Or)

(b) Write in detail about the factors involved in designing an I/O system.

V (a) Write in detail about the working of the interconnection networks.

(Or)

(b) Explain about:
(i) Distributed shared memory architecture
(ii) Synchronization mechanism.

$(4 \times 15 = 60)$

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