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Name..............................
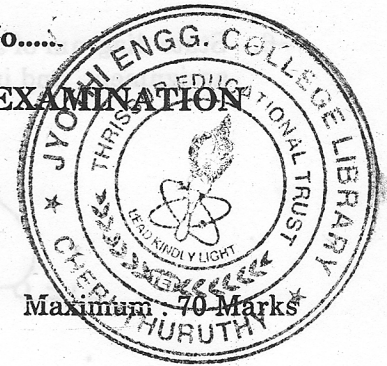
Reg. No.............

FIFTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION OCTOBER 2011

EE/PTEE 09 505—DIGITAL SYSTEM DESIGN

(2009 Admissions)

Time : Three Hours

Maximum : 70 Marks

Part A

1. Write the VHDL code for a 2 input XOR gate.

2. Where is GENERATE Statement used ?

3. What are Combinational Multiplexers ?

4. Differentiate between state table and state diagram. Which representation is best ? Why ?

5. What is meant by race free assignment ?

(5 × 2 = 10 marks)

Part B

1. With example explain package declaration in VHDL.

2. Write the VHDL code for a 2-to-1 multiplexer using SELECT signal Assignment.

3. List the rules that are useful in performing bubble–to–bubble logic design.

4. Draw the state machine structure of Mealy Machine and Moore machine.

5. Explain the I/O block of XC 9500 CPLD.

6. Draw the ASM chart for MOD–5 counter.

(4 × 5 = 20 marks)

Part C

1. (a) Explain the various steps in a VHDL based design flow. (5 marks)

   (b) Using VHDL wait statement, write code to generate input waveforms in a test–bench program. (5 marks)

Or

2. With suitable examples discuss the various data flow design elements.

3. Write a VHDL program for 8 to 1 mux and use it as a component for realization of 64 to 1 mux.

Or

4. Discuss the salient features of combinational logic timing diagram and propagation delay.

5. Design a synchronous sequential circuit that functions as a sequence detector to detect a sequence of 110011 using D flip flop.

Or

Turn over

6. State diagram of a simple sequential circuit is shown below. Construct state table, perform state assignment, and implement the circuit using D flip flops.
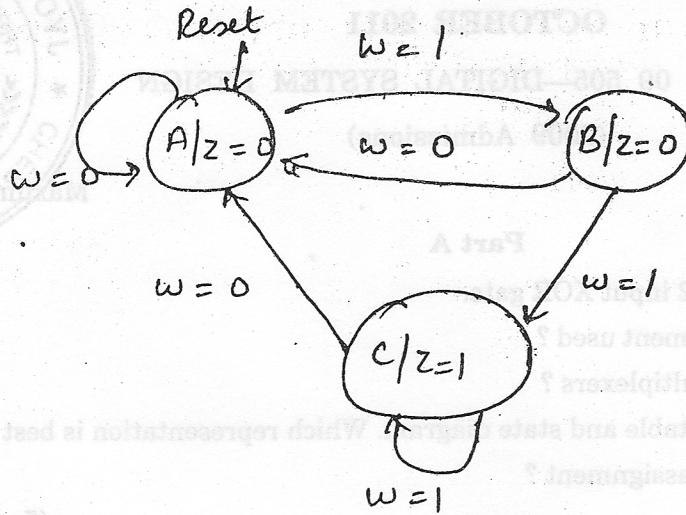
7. Discuss the analysis of circuits with multiple feedback loops with example.

Or

8. Explain the architecture of XC4000 FPGA CLB.

(4 × 10 = 40 marks)