D 8492

(Pages 2)

Name.....

Reg. No.....

FIFTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, DECEMBER 2010

EE 04 503 PULSE AND DIGITAL ELECTRONICS

Time : Three Hours

Maximum : 100 Marks

I. (a) Explain Miller Sweep circuit using op-amp.

(b) Explain forward and reverse recovery of diodes.

(c) Explain Multiplexer with a neat diagram.

(d) Explain half-adder and draw its logic diagram.

(e) Draw the excitation table and Truth table for JK flip-flop.

(f) Explain Dynamic RAM with a neat diagram.

(g) Write any *five* multibyte instructions.

(h) Explain control bus with a neat diagram.

(8 × 5 = 40 marks)

II. (a) (i) Explain resistive and clamped inductive switching of BJT. (8 marks)

(ii) Explain collector coupled Astable transistor Schmitt Trigger circuit with a neat diagram. (7 marks)

Or

(b) Explain the switching behaviour of diode with a neat diagram. (15 marks)

III. (a) (i) Reduce the following function using K-map technique :

$$f(A, B, C, D) = \sum m(0, 1, 4, 8, 9, 10).$$

(8 marks)

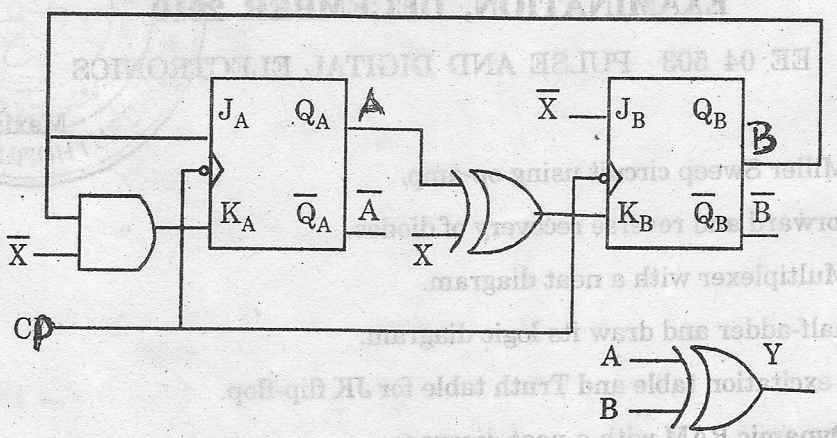
(ii) Define PLA and compare PLA with PAL. (7 marks)

Or

(b) Explain Mux and Demux with an example. (15 marks)

Turn over

IV. (a) Derive the state table and state diagram for sequential circuit shown in figure.



(15 marks)

Or

(b) (i) Draw the Excitation table and truth table of JK flip-flop. (8 marks)

(ii) Explain Johnson counter with a neat diagram. (7 marks)

V. (a) Explain the architecture of 8085 with a neat diagram.

Or

(b) (i) Write short notes on flags in 8085 processor. (8 marks)

(ii) Explain arithmetic logic unit with a neat diagram. (7 marks)

[4 × 15 = 60 marks]