

THIRD SEMESTER B.TECH. (ENGINEERING) EXAMINATION, OCTOBER 2011

EC 09 305 PTEC 09 304 DIGIT

DIGITAL ELECTRONICS

(2009 admissions)

Time: Three Hours

Maximum: 70 Marks

Part A

Answer all questions.

- 1. Generate EX-OR functions using only NOR gates.
- 2. Simplify the Boolean function using 4-variables map:

 $F(A, B, C, D) = \Sigma(0, 1, 2, 4, 5, 7, 11, 15).$

- 3. Convert the hexadecimal number F3A7C2 to binary.
- 4. Draw the simple SR latch.
- 5. What is meant by a sequential circuit?

 $(5 \times 2 = 10 \text{ marks})$

Part B

Answer any four questions.

6. Convert the following expression into sum of products and product of sums:—

 $(AB + C)(B + \overline{C}D)$.

- 7. Draw the logic diagram of 4×1 multiplexer.
- 8. Explain the working principle of TTL NAND gate.
- 9. Construct a 4-bit bidirectional shift register.
- 10. Simplify using 5-variable map:

 $F(A, B, C, D, E) = \Sigma(0, 1, 4, 5, 16, 17, 21, 25, 29).$

11. What is Mealy and Moore model?

 $(4 \times 5 = 20 \text{ marks})$

Part C

Answer section (a) or section (b) of each question.

12. (a) Simplify using Quine-Mc Cluskey method:

 $P(A, B, C, D, E, F, G) = \Sigma(20, 28, 38, 39, 52, 60, 102, 103, 127).$

| | (b) | (b) (i) Design a combinational circuit with three inputs x, y and z and three outputs A,B and When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input When the binary input is 4, 5, 6 or 7, the binary output is one less than the input. | | |
|-----|-------|--|---|------------------------------------|
| | | | | (6 marks) |
| | | (ii) | Give example for Maxterm and Minterm expansions. | (4 marks) |
| 13. | (a) | (a) Draw the logic diagram of 4-bit full adder with look ahead carry and explain the operation | | |
| | | | 406 00 DEPS | (10 marks) |
| | | | $c_{\mathrm{amp}}Or_{\mathrm{min}}$ (2.08) | |
| | (b) | Ex | plain the operation of emitter coupled logic with neat diagram. | (10 marks) |
| 14. | (a) | Co | nstruct a 4-bit updown counter with T-flip flops. | (10 marks) |
| | | , , | Or | |
| | (b) | Ex | plain SISO, SIPO, PISO and PIPO shift registers. | (10 marks) |
| 15. | (a) | (i) | Design a counter with the following repeated binary sequence, usin 0, 1, 2, 4, 6. | ng D flip-flops : |
| | | | $(2.2,2.2,2.3) \leq 0$ | (5 marks) |
| | | (ii) | Construct a MOD-10 counter. | (5 marks) |
| | | | Or . Admit 10 | 4 Dens die simple |
| | (b) | (i) | Explain the design of simple synchronous machines with example. | (6 marks) |
| | HITL. | (ii) | Explain how ASM chart differs from a conventional flowchart. | (4 marks) |
| - | | | | $[4 \times 10 = 40 \text{ marks}]$ |