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Name.....

Reg. No.....

FIFTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION OCTOBER 2011

EC/PTEC 09 501—DIGITAL SIGNAL PROCESSING

(2009 admissions)

Time : Three Hours

Maximum : 70 Marks

Part A

1. Write the shifting property of Discrete Fourier series.
2. Define DTFT.
3. What is quantization error ?
4. What is Gibb's phenomenon ?
5. What are the special instructions for DSP ?

(5 × 2 = 10 marks)

Part B

Answer any **four** *questions.*

1. Find the linear convolution of two sequences $x(n) = \{1, 2, 3, 4\}$ and $h(n) = \{1, 2, 3\}$ using graphical method.
2. Explain about filtering of long data sequences.
3. Explain how scaling is used to prevent overflow.
4. Explain truncation error for sign magnitude representation.
5. Derive the expression for frequency response of a causal FIR filter with linear phase shift.
6. Explain extended parallelism.

(4 × 5 = 20 marks)

Part C

Answer **all** *questions.*

1. Explain radix-2 decimation in time FFT algorithm.

Or

2. Find the circular convolution of the sequences $x_1(n) = \{1, 1, 2, 2\}$ and $x_2(n) = \{1, 2, 3, 4\}$ using DFT and IDFT.
3. Determine the direct forms I and II for the second order filter given by :

$$y(n) = 2b\cos(w_o)\, y(n-1) - b^2\, y(n-2) + x(n) - b\cos(w_o)\, x(n-1)$$

Or

4. Explain the coefficient quantization effects in direct form realization of IIR filters and draw the coefficient quantization model for direct from realization of IIR filter.

Turn over

5. A low pass filter has the desired frequency response as give below :

$$H_d(e^{jw}) = \begin{cases} e^{-j3w}, & 0 \le w < \frac{\pi}{2} \\ 0, & \frac{\pi}{2} \le w \le \pi \end{cases}$$

Determine the filter coefficients $h(n)$ for M = 7 using type-I frequency sampling technique.

Or

6. Design a digital Butterworth filter satisfies the following constraint using bilinear transformation. Assume T = 1 sec.

$$0.9 \le |H(e^{jw})| \le 1, \quad 0 \le w < \frac{\pi}{2}$$

$$|H(e^{jw})| \le 0.2, \quad \frac{3\pi}{4} \le w \le \pi$$

7. Explain the basic multiplier and MAC unit DSP computational building blocks in detail.

Or

8. Explain the different data addressing modes of TMS320 series processor.

(4 × 10 = 40 marks)