D 8479

Name.....

Reg. No.....

FIFTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, DECEMBER 2010

EC 04-503—LINEAR INTEGRATED CIRCUITS

Time : Three Hours Maximum : 100 Marks

Answer **all** *questions.*

1. (a) What is a level translator ? Where is it used in 741 op-amp ? Explain.

   (b) Draw the circuit of op-amp differentiator and obtain expression for output voltage.

   (c) Explain the circuit of op-amp based analog multiplier.

   (d) Design the RC elements of a Wien bridge oscillator for operation at f_0 = 1 kHz. Draw the circuit.

   (e) Draw the Twin-Tee Notch filter and explain.

   (f) Explain the basic principle of high current voltage regulator.

   (g) Draw the functional diagram of 566.

   (h) What are the drawbacks of dual slope ADC ? Explain briefly.

   (8 × 5 = 40 marks)

2. (a) Discuss the various a.c. and d.c. parameters of op-amp and their significance.

   Or

   (b) Construct and explain :

   (i) Logarithmic amplifier using op-amp.

   (ii) Integrator.

3. (a) Design a 2nd order LCR resonator and explain.

   Or

   (b) Draw the circuit of a 2nd order switched capacitor based LPF and explain its operation.

4. (a) Explain the LM 723 voltage regulator with functional diagram.

   Or

   (b) Discuss the working of R-2R type DAC.

5. (a) (i) The lock range of PLL is specified to be ± 15 % of center frequency. Determine the minimum and maximum frequencies for which PLL will maintain lock if f_0 = 50 kHz.

   (5 marks)

   (ii) Explain the operation of VCO. (10 marks)

   Or

   (b) (i) Draw the block diagram of frequency synthesizer and explain how it is implemented using IC 565 PLL unit.

   (ii) Discuss the block diagram of 555 timer and its operation in Astable model.

   (4 × 15 = 60 marks)