D 20628-A (Pages : 2) Name.....................................

Reg. No.....................................

THIRD SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, OCTOBER 2011

CS/IT 09 306/PTCS 09 305—SWITCHING THEORY AND LOGIC DESIGN

(2009 admissions)

Time : Three Hours Maximum : 70 Marks

Part A

Answer **all** *questions.*

1. Convert $(342.45)_{10}$ to binary and Octal.
2. What is prime implicant ?
3. What is the difference between decoder and demultiplexer ?
4. What are the terms that determines the size of a PLA ?
5. What is meant by race around condition ?

(5 × 2 = 10 marks)

Part B

Answer any **four** *questions.*

6. Write short note on weighted code.
7. Explain how can AND-OR circuit can be converted to NAND and NOR logic.
8. Explain 1 of 8 demultiplexer with neat logic diagram.
9. Explain briefly different types of ROMs.
10. Determine the Boolean difference for the following functions :—

    $Y_1 = AB + AC + BC$

    $Y_2 = (A + B)(A + C)(B + C)$.
11. Draw the logic diagram of a 3 bit binary ripple counter using toggle flip-flops.

(4 × 5 = 20 marks)

Part C

12. (a) (i) Use Karnaugh map to simplify the function $F = AB + A(B + C) + B(B + C)$. (5 marks)

    (ii) Implemen the function $Y = AB + \overline{A}\overline{B} + \overline{B}C$ with OR and inverter gates. (5 marks)

    Or

    (b) Simplify the following Boolean function by using Quine McCluskey mehtod :

    $F(A, B, C, D) = \Sigma m(0, 2, 3, 6, 7, 8, 10, 12, 13)$.

Turn over

13. (a) Design a logic circuit to convert excess-3 code to BCD code.

Or

(b) (i) Design a full adder usign only NOR gates. (5 marks)

(ii) Draw the logic diagram of decimal to BCD encoder and explain its working. (5 marks)

14. (a) Derive a test set that can detect all single faults in the 2 to 4 decoder with enable input.

Or

(b) Explain folding of PLA with examples.

15. (a) (i) Draw the logic diagram of JK flip-flop and explain its function with truth table. (5 marks)

(ii) Explain the working of serial-in-parallel out shift register with logic diagram. (5 marks)

Or

(b) Design a sequential logic circuit with two D-flip-flops, A and B and one input x, when $x = 0$, the state of the circuit remains the same. When $x = 1$, the circuit passes through the state transitions from 00 to 01 to 11 to 10 and back to 00 and repeats.

[4 × 10 = 40 marks]