23186

Name: .....

Reg. No. .....

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SEVENTH SEMESTER B.TECH. DEGREE EXAMINATION, DECEMBER 2011

AI 04.703 – Digital MOS Circuits (2004 Admissions)

Time: Three hours **Maximum : 100 marks**

I. (a) Compare MOS and BJT families.

(b) Explain in detail about enchancement and depletion MOSFETs.

(c) Design a resistive load inverter for V_{DD}=3.3 V, V_{OL}= 0.15 V, β_n' = 60 μV/V². Assume I_d=30 μA at inverter switching threshold and the value of switching threshold of the inverter is 1.5 V.

(d) What is a Super buffer? Explain with its schematic.

(e) What is a transmission gate? Design a 4x1 Multiplexer using Transmission gates.

(f) With schematic explain the operation of a BICMOS inverter.

(g) Explain the features of NORA Logic and compare it with static CMOS.

(h) What is an adiabatic logic? Explain.

(8 × 5 = 40 marks)

II. (a) Discuss in detail about the second order effect of MOS.

(or)

(b) With neat sketch explain the structure of a MOSFET and its small signal and large signal parameters.

III. (a) Derive an expression for the V_{OH}, V_{IH}, V_{IL} and V_{OL} of a resistive load inverter

(or)

(b) (i) Derive an expression for the power dissipation of a CMOS inverter.

(ii) Derive an expression for the propagation delay of a CMOS inverter.

IV. (a) Draw the transistor level schematic of a CMOS NOR and NAND gates and explain their operation.

(or)

(b) (i) Implement a F= AB and F=A+B using Pass transistor logic

(ii) Explain the Boot strapping and its advantages.

V. (a) Discuss in detail about the two phases of operation of a Dynamic CMOS logic and its advantages and disadvantages over Static CMOS logic.

(or)

(b) (i) What is charge sharing in Domino Logic? How it is avoided

(ii) Realize the following function using Domino Logic:

F= AB + CD

[4 × 15 = 60 marks]