D 20631 (Pages : 2) Name.....

Reg. No.....

THIRD SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION OCTOBER 2011

AI 09 305—DIGITAL SYSTEMS

(2009 Admissions)

Time : Three Hours Maximum : 70 Marks

Part A

Answer **all** *questions.*

1. State consensus theorem.
2. Simplify $f = AB + BC + B'C'$.
3. State the advantage of carry look-ahead adders.
4. Implement the following function using AND-OR realization $f = ABC + A'BC'D$.
5. Define fan-in and fan-out.

(5 × 2 = 10 marks)

Part B

Answer any **four** *questions.*

6. Implement the following function using SOP and POS forms

$$f(A, B, C) = AB + AC + A'C' + A'B' + A'B + AC'$$

7. Simplify the following function

$$f(A, B, C, D) = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 11, 12)$$

8. Design a full Adder.
9. Design a 2-bit magnitude comparator.
10. Design a 2-bit Asynchronous counter using JK flip flops.
11. Explain the basic principle of partitioning procedure.

(4 × 5 = 20 marks)

Part C

Answer Section (a) **or** *Section (b) in each questions.*

12. (a) The Hamming Code 101101101 is received. Correct it if any errors. There are four parity bits and odd parity is used.

Or

(b) Simplify the following function using Quine Mc Cluskey method

$$f(A, B, C, D, E) = \sum m(0, 1, 2, 3, 5, 7, 9, 12, 15, 17, 21, 25, 27, 29, 30, 31)$$

Turn over

13. (a) Design a BCD adder.

Or

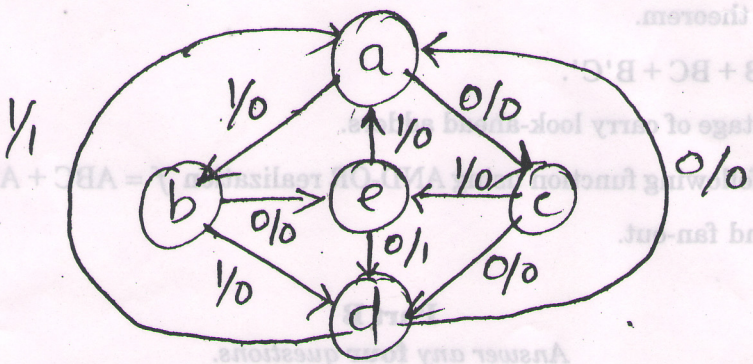
(b) What is a race around condition ? How it is avoided in Master Slave JK flip flop ? Explain.

14. (a) Design a 4-bit universal shifter and explain its operation.

Or

(b) Draw the circuit schematic of a 2-input TTL NAND gate and explain its operation.

15. (a) Design a Sequential circuit for the state diagram shown in figure. Use state assignment rules for assigning states.



Or

(b) Design a sequence recogniser to detect the sequence 1011.

(4 × 10 = 40 marks)