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THIRD SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION OCTOBER 2011

AI 09 303—ELECTRONIC CIRCUITS—I

(2009 Admissions)

Time : Three Hours Maximum : 70 Marks

Part A

1. What is a PN Junction diode ? How its terminals are identified ?
2. The Q-factor of a 100 mH inductor is 80. When operated in 400 kHz range. What is the d.c. resistance (R_0) of the inductor ?
3. What is the function of a bleeder resistor ?
4. Name different types of biasing circuits and give three circuit configurations.
5. How do you set a Q-point in a self-biased JFET ?

(5 × 2 = 10 marks)

Part B

6. How does the dynamic resistance r of a diode vary with (a) Current and (b) Temperature (c) What is the order of magnitude of r for silicon at room temperature and for a de current of 1mA ?
7. A zener diode voltage regulating circuit is an shown if Fig. 1. The zener diode used has zener Voltage (V_z) of 15V and minimum current I_z (min) of 2μA, a power dissipation of 120 mW and a zener resistance of 40Ω. If the load resistance is 5KΩ and the input voltage varies from 18 to 24V, find the value of R_s.

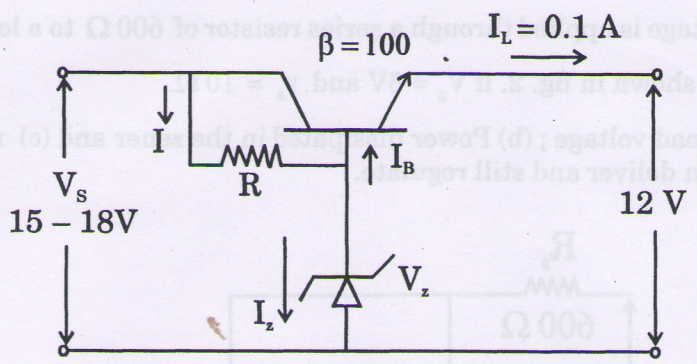

Fig. 1.

8. What are the advantages of a bridge rectifier as compared to a full wave center-tapped rectifier ?
9. Compare the relative stability of (a) emitter bias and fixed bias circuit, (b) emitter bias and voltage divide bias circuits.

Turn over

10. Explain the essential difference between the RC coupled and direct coupled amplifier.

11. A certain JFET amplifier has g_m of 4ms, r_d = 10KΩ and R_D = 5KΩ. What is the voltage gain ? Assume the source resistance to be zero.

(4 × 5 = 20 marks)

Part C

12. A.(i) (a) Draw the piecewise linear voltampere characteristic of a p-n diode.

(b) What is the circuit model for the ON state ?

(c) The OFF state. (6 marks)

(ii) (a) Derive the expression for I_C versus I_B for a CE transistor configuration in the active region.

(b) For I_B = 0, What is I_C ? (4 marks)

Or

B.(i) (a) Sketch the circuit of a CS amplifier.

(b) Derive the expression for the voltage gain at low frequencies.

(c) What is the maximum value of A_V ? (6 marks)

(ii) (a) Sketch the cross section of a *p*-channel enhancement MOSFET.

(b) Show *two* circuit symbols for this MOSFET.

(4 marks)

13. A. Draw the circuit diagram of a full wave rectifiers :

(a) With center-tap connection and

(b) Bridge connection. Explain their working.

What is the peak inverse voltage of a diode in each case ? (10 marks)

Or

B. (i) Draw circuit diagram of transistor shunt regulator. Explain it briefly.

(5 marks)

(ii) A 36 V d.c Voltage is applied through a series resistor of 600 Ω to a load 300 Ω shunted by a zenerdiode as shown in fig. 2. if V_z = 8V and γ_z = 10 Ω.

Find (a) d.c. Load voltage ; (b) Power dissipated in the zener and (c) maximum current, that a regulator can deliver and still regulate.

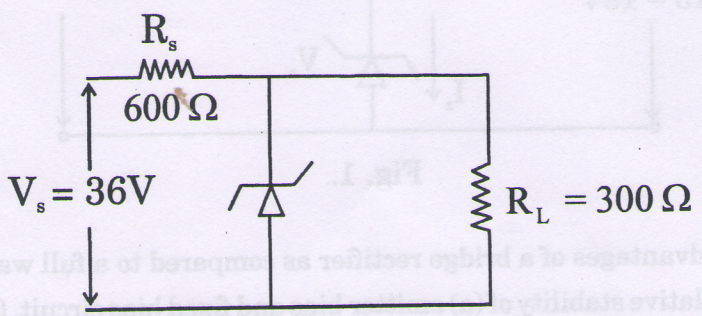

Fig. 2.

(5 marks)

14. A. (i) Derive an expression for the stability factor of a fixed bias current. (4 marks)

(ii) Draw a voltage divider bias circuit and derive an expression for its stability factor. (6 marks)

Or

B. Derive the expressions for input resistance, output resistance, current gain and voltage gain of a common emitter amplifier. (10 marks)

15. A. (i) What are the biasing schemes available to achieve the required bias in a JFET ? Explain any one of the biasing schemes. (6 marks)

(ii) A certain JFET has a transconductance (g_m) of 2500 μS. With an external drain resistance of 2kΩ. Find the value of ideal voltage gain. (4 marks)

Or

B. (a) Sketch the small signal high frequency circuit of a CS amplifier.

(b) Derive the expression for the voltage gain. (10 marks)