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Name.....

Reg. No.....

FIFTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION DECEMBER 2010

AI/BM 04 504—COMPUTER ORGANIZATION AND ARCHITECTURE

Time : Three Hours Maximum : 100 Marks

I. (a) What are the two addressing modes available to access the variables ?

(b) With an example, explain the subroutine stack frame.

(c) Give the equivalent circuit for an open-drain bus used to implement a common interrupt request line.

(d) Briefly explain the functions of a memory controller.

(e) What is the effect of an execution operation taking more than one clock cycle ?

(f) What are Graphic Accelerators ? Write a note on it.

(g) Give the classification of pipeline processors.

(h) Briefly explain the SIMD Array processor.

(8 × 5 = 40 marks)

II. (a) Explain in detail about the various addressing modes.

Or

(b) Explain in detail about :

(i) Logical shift.

(ii) Arithmetic shift ; and

(iii) Rotate

instructions.

III. (a) Discuss in detail about the semiconductor RAM memories.

Or

(b) With the sequential circuit, explain the operation of a binary multiplier.

IV. (a) Explain in detail about :

(i) Data Hazards.

(ii) Instruction Hazards.

Or

(b) Explain in detail about the superscalar processors.

V. (a) Briefly explain the following architectural classification schemes :

(i) Flynn's classification.

(ii) Feng's classification.

(iii) Handler's classification.

Or

(b) Explain in detail about the bandwidth balancing mechanisms between CPU, memory and I/O systems in a uniprocessor computer.

(4 × 15 = 60 marks)