C 5486 (Pages 2) Name.....

Reg. No.....

SEVENTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, JUNE 2010

AI 04 703—DIGITAL MOS CIRCUITS

(2004 Admissions)

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*

1. (a) Explain about subthreshold current.

   (b) Write notes on constant field scaling of MOSFET.

   (c) Explain about pseudo NMOS logic.

   (d) Explain about the estimation of interconnect parasitics.

   (e) Write notes on Transmission gate and pass transistor logic.

   (f) Write notes on BiCMOS switching transients.

   (g) Realise $f = \overline{A + B}$ using domino logic.

   (h) Write notes on NORA logic.

(8 × 5 = 40 marks)

Part B

2. (a) Write notes on :

   (i) Channel length modulation.

   (ii) Hot electron effects.

   (iii) Digital MOSFET model.

Or

   (b) Write notes on :

   (i) Drain induced barrier lowering.

   (ii) Constant voltage scaling of MOSFET.

3. (a) (i) Explain the working of CMOS inverter.

   (ii) Calculate the delay times of CMOS inverter.

Or

(b) (i) Design and explain the working of super butter.

(ii) Write notes of CMOS ring oscillator.

4. (a) Design and explain the working of SR and JK latches using CMOS logic.

Or

(b) (i) Explain the working of BiCMOS inverter.

(ii) Explain the working of a two input BiCMOS NAND gate.

5. (a) Explain on :

(i) NOR A logic.

(ii) Precharge/evaluate logic.

Or

(b) (i) Explain about adiabatic logic.

(ii) Explain about true single phase clock dynamic logic.

(4 × 15 = 60 marks)