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Name .....

Reg. No.....

VIII SEMESTER B.TECH DEGREE EXAMINATION JUNE 2010

C S 04 802 COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

Time : 3 Hours Max. marks : 100

(Answer All Questions)

(8 × 5 = 40 marks)

I. 1) Discuss the various technologies that changes dramatically which leads to a critical problem for a modern implementation.

2) Define Amdahl's Law and explain the two factors which give the enhancement for speed.

3) What is Instruction Level Parallelism? Explain.

4) Give the expansion for RAW, WAW, WAR and explain briefly.

5) Write the first optimization of cache performance and explain how it will reduce hit time.

6) Draw and explain the multilevel memory hierarchy. For what purpose the memory hierarchy will be helpful for the user.

7) Why the coherence and consistency are complementary? Explain.

8) What is meant by snooping? Write the different protocols used in snooping protocols.

II. (a) Define Benchmark. How the benchmarks will be the best choice to measure the performance of a real applications and give the examples for pitfalls in real applications. (15)

(or)

b) (i) What is pipelining? Write the formula to perfectly balance the pipeline stage. (4)

(ii) Draw and explain the Data hazard and stalls. How the data hazard stalls is minimized using the forwarding technique. (11)

III. (a) (i) What is the difference between the pipeline and the Scheduling? How many clock cycles will take for the 4 Byte instructions? (5)

(ii) How the Data Hazard will overcome the Dynamic Scheduling (10)

(or)

(b) Explain the Vector architecture with suitable examples and diagrams. (15)