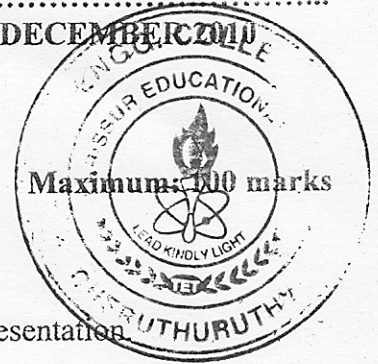


## FOURTH SEMESTER B.TECH. DEGREE EXAMINATION, DECEMBER 2011

## EC.04.403 – Digital Electronics

Time: Three hours



- I. a) State and prove De Morgan's theorem.  
 b) Perform the following subtractions using 2's complement representation.  
 i)  $25_{10} - 12_{10}$   
 ii)  $16_{10} - 8_{10}$   
 c) Define the following terms  
 i) Noise Margin  
 ii) Propagation delay  
 iii) Power dissipation  
 d) Deduce the characteristic equation of the JK flip flop and draw the logic circuit.  
 e) State the differences between Mealy and Moore state models.  
 f) What are the basic building blocks of an ASM chart? Explain.  
 g) What is static 0 and 1 hazard? Give examples.  
 h) State the rules for state assignment.

(8 × 5 = 40)

- II. a) Reduce the following expression using Karnaugh Map  

$$F(A, B, C, D) = \sum M(0, 2, 4, 6, 8, 10) + \sum d(1, 3, 5)$$
  
 (Or)  
 b) Reduce the following expression using Quine McCluskey method.  

$$F(A, B, C, D, E) = \sum m(0, 2, 5, 9, 11, 12, 17, 25, 31)$$

- III. a) Draw and explain the operation of a two Input TTL Nand gate.  
 (Or)  
 b) What is race around condition? How it is avoided in Master slave JK flip flop? Explain.

- IV. a) Design a sequential Serial Adder using  
 i) Mealy State Model  
 ii) Moore State Model  
 (Or)  
 b) Explain the partitioning procedure for state minimization with a suitable example.

- V. a) Discuss in detail about the steps involved in the analysis and Synthesis of Asynchronous sequential circuits.  
 (Or)  
 b) With an example explain the following types of asynchronous sequential circuits in detail.  
 i) Pulse Mode circuits.  
 ii) Fundamental Mode circuits.

(4 × 15 = 60)

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