C 14712 (Pages : 2) Name.....

Reg. No.....

SIXTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, DECEMBER 2010

EC/AI/IC/BM 04 602—DIGITAL SIGNAL PROCESSING

Time : Three Hours Maximum : 100 Marks

Answer all *questions.*

Part A

1. (a) Find the 4-point DFT of $x(n) = \{0, -2, 4, -6\}$.

(b) What is the need for FFT algorithm ? State the computational requirements of radix 2 FFT algorithm.

(c) Explain how will you develop cascade structure with direct form realization.

(d) Explain what is meant by zero-input limit cycle.

(e) Explain the desirable features of window functions for designing FIR filter.

(f) Explain matched z-transformation for IIR filter design.

(g) Draw the block diagram of basic Harvard architecture and explain.

(h) Explain about hardware multiplier-accumulator.

($8 \times 5 = 40$ marks)

Part B

2. (a) (i) Explain how do determine linear filtering of longer data using DFT. (8 marks)

(ii) Explain the frequency analysis of discrete-time signals using DFT. (7 marks)

Or

(b) (i) Explain divide and conquer approach to computation of the DFT. (10 marks)

(ii) Using FFT, find the inverse DFT of $X(K) = \left\{1, 1-j\sqrt{2}, 1, 1+j\sqrt{2}\right\}$. (5 marks)

3. (a) (i) Derive the relationship between direct form FIR coefficients and lattice coefficients. (9 marks)

(ii) Obtain direct form FIR coefficients corresponding to the lattice coefficients : $K_1 = 0.65$, $K_2 = -0.34$. (6 marks)

Or

(b) (i) The output of an A/D converter is applied to a digital filter with the system function :

$$H(z) = \frac{0.5z}{z - 0.5}.$$

Turn over

Find the output noise power from the digital filter, when the input signal is quantized to have eight bits.

(7 marks)

(ii) Explain the method of scaling to prevent overflow limit oscillations. (8 marks)

4. (a) (i) Design a linear phase FIR band-pass filter with lower and upper cut-off frequencies at 0.2 rad/sec. and 0.3 rad./sec. respectively using Hanning window of length 15.

(8 marks)

(ii) Derive the frequency response of linear phase FIR filter of order N (odd) with antisymmetric impulse response.

(7 marks)

Or

(b) (i) Derive bilinear transformation mapping formula for designing IIR digital filter.

(7 marks)

(ii) Convert the following analog filter into digital using impulse invariant mapping technique. Assume T = 1 sec.

$$H(s) = \frac{s+0.2}{(s+0.2)^2+9}.$$

(8 marks)

5. (a) (i) Explain the principles of superscalar architecture and data flow in DSP processor.

(7 marks)

(ii) Explain the implementation of FIR filtering on DSP processor. (8 marks)

Or

(b) (i) Draw the block diagram of architecture of a second generation fixed point DSP processor and explain.

(9 marks)

(ii) Explain a simplified architecture of a hardware FFT processor. (6 marks)

[4 × 15 = 60 marks]