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Name.....

Reg. No.....

FOURTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, DECEMBER 2010

EC 04 404 – COMPUTER ORGANISATION AND ARCHITECTURE

(2004 Admissions)

Time : Three Hours Maximum : 100 Marks

Answer questions as per choice.

1. (a) Compare structural versus behavioural description of any system.
   (b) With a flow diagram give an overview of CPU behaviour.
   (c) Draw and explain a serial binary adder.
   (d) Explain with the tuning diagram the four-phase of a microinstruction.
   (e) Draw the common memory hierarchies and give a brief explanation about them.
   (f) Write the general approach used to design the cache's main size parameter K, S_1, P_1.
   (g) Explain the single shared bus architecture of computer communication.
   (h) Explain bus arbitration using independent requesting.

(8 × 5 = 40 marks)

2. (a) Design sixteen-input multiplexers using two-input multiplexers.

Or

   (b) Explain how instructions and data are formatted for a computer system.

3. (a) Explain the working of a pipelined multiplier.

Or

   (b) Explain the basic structure of a microprogrammed control unit.

4. (a) Explain the various characteristics of memory devices.

Or

   (b) Explain the design of 256 kB direct mapped cache for a microprocessor.

5. (a) Explain with a block diagram the DMA method of IO control.

Or

   (b) Explain the organization of a IO processor.

(4 × 15 = 60 marks)