15648

Name: .....

Reg.No.: .....

FOURTH SEMESTER B.TECH. DEGREE EXAMINATION, JUNE 2011

EC.09.405/PTEC.09.404 – Computer Organization and Architecture
(2009 Admission)

Part A

(5 x 2 Marks=10 Marks)

1. What are the three levels at which the design of a computer can be carried out?
2. What are bench marks?
3. State Kerr effect.
4. What is a computer network? State any two of its advantages.
5. What is an interrupt?

Part B

(4 x 5 Marks = 20 Marks)

6. With flow chart, explain an iterative design process.
7. Explain the steps involved in the program execution.
8. With the conceptual model diagram, explain the random access memory.
9. With timing diagram, explain the synchronous data transfer.
10. Explain the four broad groups of computers given by Flynn's classification.
11. Write a note on Push and Pop operation in a stack.

Part C (4 x 10 = 40 Marks)

12. (i) With block diagram, explain the processor memory communication with and without a cache memory. (5)

    (ii) With flow chart and programming considerations, explain the CPU operation. (5)

(or)

13. Explain in detail about

    (i) Combinational ALU and (ii) Sequential ALU (10)

14. Discuss in detail about the common memory hierarchies with two, three and four levels. (10)

(or)

15. Discuss in detail about Associative and Set Associative addressing modes. (10)

16. Explain the following interconnection structures and compare them in terms of number of edges, maximum node degree and maximum internode distance : (10)

(i) Linear (ii) Mesh (iii) ring (iv) Star (v) hypercube

(or)

17. Discuss in detail about the Direct Memory Access (DMA) and Interrupts. (10)

18. Draw the functional block diagram of 8085 and explain the function of each of its blocks. (10)

(or)

19. Discuss in detail about

(i) Memory Mapped I/O

(ii)I/O Mapped I/O (10)

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