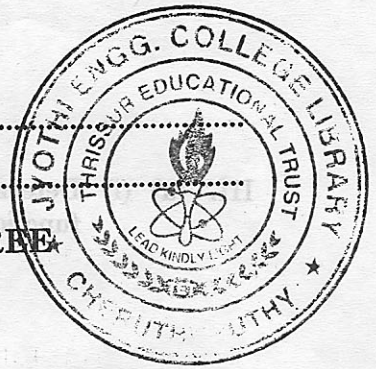


C 6117

(Pages : 2)

Name.....

Reg. No.....



**SIXTH SEMESTER B.TECH. (ENGINEERING) DEGREE  
EXAMINATION, JUNE 2010**

**EC/AI/IC/BM 04 602—DIGITAL SIGNAL PROCESSING  
(2004 admissions)**

Time : Three Hours

Maximum : 100 Marks

Answer all questions.

**Part A**

- I. (a) State and prove any two properties of DFT.  
(b) Explain the efficient computation of the DFT of two real sequence using FFT algorithm.  
(c) A digital system is described by the difference equation

$$y(n) = 0.9y(n-1) + x(n)$$

with  $x(n) = 0$  and initial condition  $y(-1) = 12$ . Determine the dead-band of the system.

- (d) Obtain direct-form and cascade form realizations for the system function of an FIR filter given by

$$H(z) = [1 - 0.25z^{-1} + (3/8)z^{-2}] [1 - 1/8z^{-1} - 0.5z^{-2}]$$

- (e) What is a linear phase filter? What conditions are to be satisfied by the impulse response of an FIR system in order to have a linear phase?  
(f) What is bilinear transformation? Explain.  
(g) What is pipelining? Explain.  
(h) Explain any two special instructions for DSP operations.

(8 × 5 = 40 marks)

**Part B**

- II. (a) (i) Find the response of an LTI system with impulse response  $h(n) = \{6, -7\}$  for the input  $x(n) = \{2, -6, -12\}$  using DFT.

(10 marks)

- (ii) Explain frequency analysis of signals using the DFT.

(5 marks)

Or

- (b) (i) Derive decimation-in-time radix-2 FFT algorithm.  
(ii) Define the following with respect to wavelet transform :

(9 marks)

(1) Mother wavelet.

(2) Continuous wavelet transform and its inverse transform.

(2 + 4 = 6 marks)

Turn over

- III. (a) (i) Determine the lattice structure corresponding to the FIR filter described by the system function :

$$H(z) = 1 + 0.9z^{-1} - 0.8z^{-2} + 0.5z^{-3}$$

(12 marks)

- (ii) What are the advantages of lattice structure over direct-form FIR structure ? (3 marks)

Or

- (b) (i) Explain coefficient quantization effects in direct-form realization of IIR filters.

(10 marks)

- (ii) Explain what is meant by limit cycle oscillations.

(5 marks)

- IV. (a) (i) Explain design of FIR filter by frequency sampling.

(8 marks)

- (ii) Explain the characteristics of practical frequency selective filters with neat diagram.

(7 marks)

Or

- (b) Design a Butterworth filter using bilinear transformation to meet the following constraints :

$$\frac{1}{\sqrt{2}} \leq |H(w)| \leq 1 \text{ for } 0 \leq w \leq \frac{\pi}{2}$$

$$0 \leq |H(w)| \leq 0.2 \text{ for } \frac{3\pi}{4} \leq w \leq \pi.$$

(15 marks)

- V. (a) (i) Draw the block diagram of basic generic hardware architecture for signal processing and explain.

(9 marks)

- (ii) Explain hardware multiplier accumulator with block diagram.

(6 marks)

Or

- (b) (i) Explain the architecture of a hardware FIR digital filter with neat diagram.

(8 marks)

- (ii) Explain the principles of very long instruction word architecture.

(7 marks)

[4 × 15 = 60 marks]